

COMPACTPCI-817 PERIPHERAL BOARD

USER'S MANUAL



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1.1 INTRODUCTION

The CPCI-817 is a high-performance CompactPCI peripheral board featuring two ATM SARs for dual E1 ATM line interface. A block diagram is shown in Figure 1-1.

The board is based on the MPC8240 PowerPC™ integrated processor. The MPC8240 has a processor core based on the PowerPC603e™ low-power microprocessor, and also performs many peripheral functions on chip. The peripheral logic integrates a PCI bridge, memory controller, DMA controller, interrupt controller, I₂O controller, and an I²C controller.

Software development tools for PowerPC processors are available from a variety of vendors, and a Board Support Package (BSP) for the pSOS operating system is available from Cyclone.

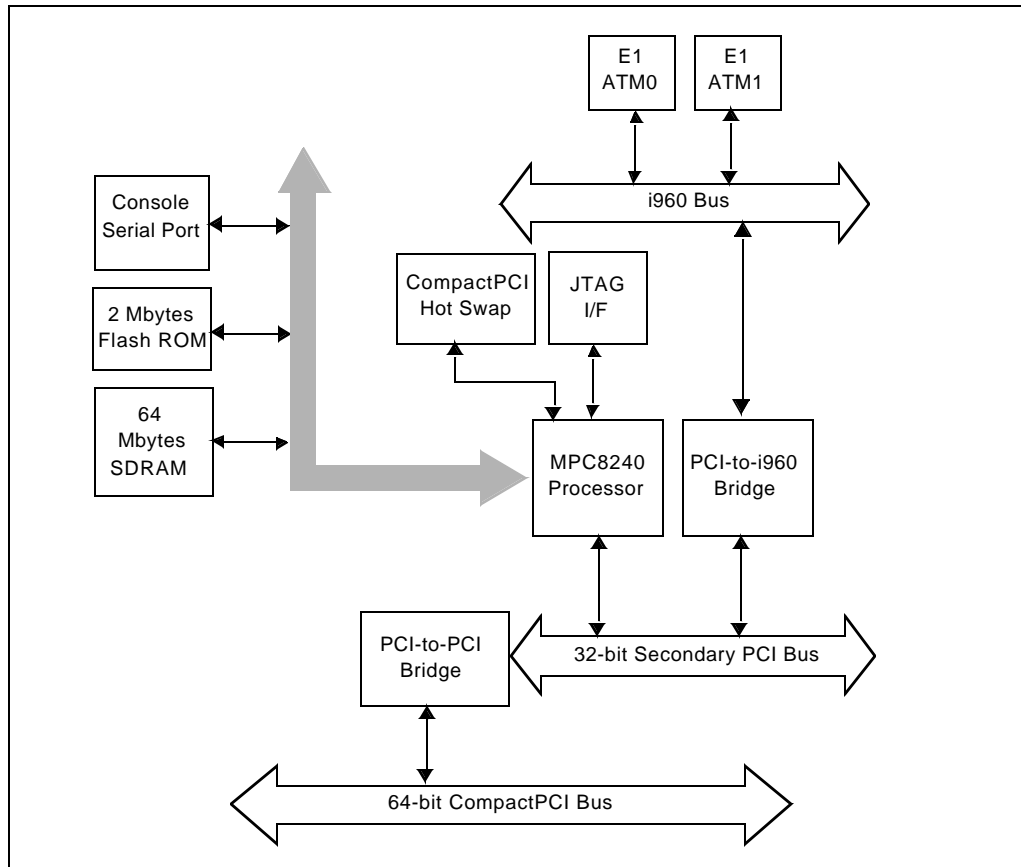


Figure 1-1. CPCI-817 Block Diagram

1.2 FEATURES

- MPC 8240 Processor

The microprocessor is Motorola's integrated MPC8240 PowerPC. The device integrates a Motorola 32-bit superscalar PowerPC 603e core, running at 250 MHz internally, and Peripheral Components Interconnect (PCI). The core boasts a 16 Kbyte instruction cache, a 16 Kbyte data cache and floating-point support. Memory can be accessed through the memory controller to the core processor or from the PCI bus.
- 21554 PCI-to-PCI Bridge

The 21554 is a "non-transparent" PCI-to-PCI bridge with a 64-bit primary bus interface and a 64-bit secondary interface. A non-transparent bridge allows the local processor to configure and control the local subsystem. The 21554 primary bus interfaces with the 64-bit CompactPCI bus and the secondary bus interfaces with the 32-bit PCI bus of the MPC8240.
- SDRAM

64 MBytes of ECC SDRAM is standard on the CPCI-817.
- *CompactPCI* Interface

The CPCI-817 meets the PICMG 2.0 Rev. 2.1 Specification for system slot adapters. The PCI bus runs at 33MHz.
- Flash ROM

2 Mbytes of in-circuit sector-programmable Flash ROM.
- Console Serial Port

An RS-232 serial port is provided for a console terminal or workstation connection. The serial port supports up to 115 Kbps and uses a phone jack to DB25 cable supplied with the CPCI-817 board.
- Hot Swap

The CPCI-817 is a Full Hot Swap board, compliant with PICMG 2.1.
- Timers

Four 31-bit timers are available to generate interrupts.
- DMA Controller

The MPC8240 supports 2 separate DMA channels for high throughput data transfers between PCI bus agents and the local SDRAM memory.
- I₂O Messaging

The CPCI-817 supports the I₂O specification for interprocessor communication.
- Hardware Segmentation

Complete hardware segmentation of user packets to ATM cells, including physical layer convergence and transmission over an E1(2.048 Mbit/s coax cable) line.
- Hardware Assembly

Complete hardware assembly of ATM cells received on an E1(2.048 Mbit/s coax cable) line into user packets.
- Memory Access

Direct memory access of packets stored in host memory for segmentation and reassembly.

1.3 OVERVIEW

The CPCI-817 is a 6U CompactPCI peripheral board with two ATM-E1 interfaces, which uses three VLSI circuits (ATM SAR, E1XC & SUNI-PDH). The ATM SAR performs hardware segmentation of user packets into ATM cells and hardware reassembly of ATM cells into user packets. The SUNI-PDH implements the mapping of ATM cells into the E1 frame structure. The E1XC provides the E1 line interface.

The CPCI-817 has two PCI buses, a primary and a secondary. The primary PCI bus is the CompactPCI bus. The secondary PCI bus is a local bus that supports the MPC8240 and PLX PCI9080 bridge, which interfaces the ATM SARs through an Intel 80960 bus.

The CPCI-817 uses an Intel 21554 Embedded PCI-to-PCI Bridge to bridge between the primary CompactPCI bus and the secondary local PCI bus. This device complies with the PCI Local Bus Specification, revision 2.1. It provides concurrent bus operation, allows buffering for both read and write transactions and provides support for Hot Swap operation.

The primary PCI interface is 64-bit data but will operate correctly when the CPCI-817 is plugged into a 32-bit CompactPCI slot. Although the secondary PCI bus of the 21554 is 64-bit data, the local bus of the CPCI-817 is 32-bit, the MPC8240 and PCI9080 are 32-bit PCI devices. The data path to memory of the CPCI-817 is 64-bit. The memory controller resides on the MPC8240.

The Flash ROM on the CPCI-817 can be reprogrammed by software through a JTAG/COP interface. Utilities to perform this programming are available from software development tool vendors. Additional information on the JTAG/COP interface can be found in section 3.10.

1.4 SPECIFICATIONS

Physical Characteristics CPCI-817 is a single slot, double high *CompactPCI*[™] peripheral card.

Height: 9.187" (233.35mm) Double Eurocard (6U)

Depth: 6.299" (160mm)

Width: .8" (20.32mm)

Power Requirements The CPCI-817 requires +5V, +12V and +3.3V from the *CompactPCI*[™] backplane J1 connector.

The following table represents the power consumption of the CPCI-817.

Table 1-1. CPCI-817 Power Requirements

Voltage	Current Typical	Current Maximum
+3.3V	2.411 Amps	3.465 Amps
+5V	2.197 Amps	3.144 Amps
+12V	0.002 Amps	0.003 Amps
-12V	0 Amps	0 Amps

1.5 ENVIRONMENTAL

The CPCI-817 should be operated in a CompactPCI card cage with good air flow. The board can be operated at ambient air temperature of 0-55 degrees Celsius, as measured at the board.

Table 1-2. Environmental Specifications

Operating Temperatures	0 to 55 Degrees Celsius
Relative Humidity (non-condensing)	0-95%
Storage Temperatures	-55 to 125 Degrees Celsius

1.6 PHYSICAL ENVIRONMENT

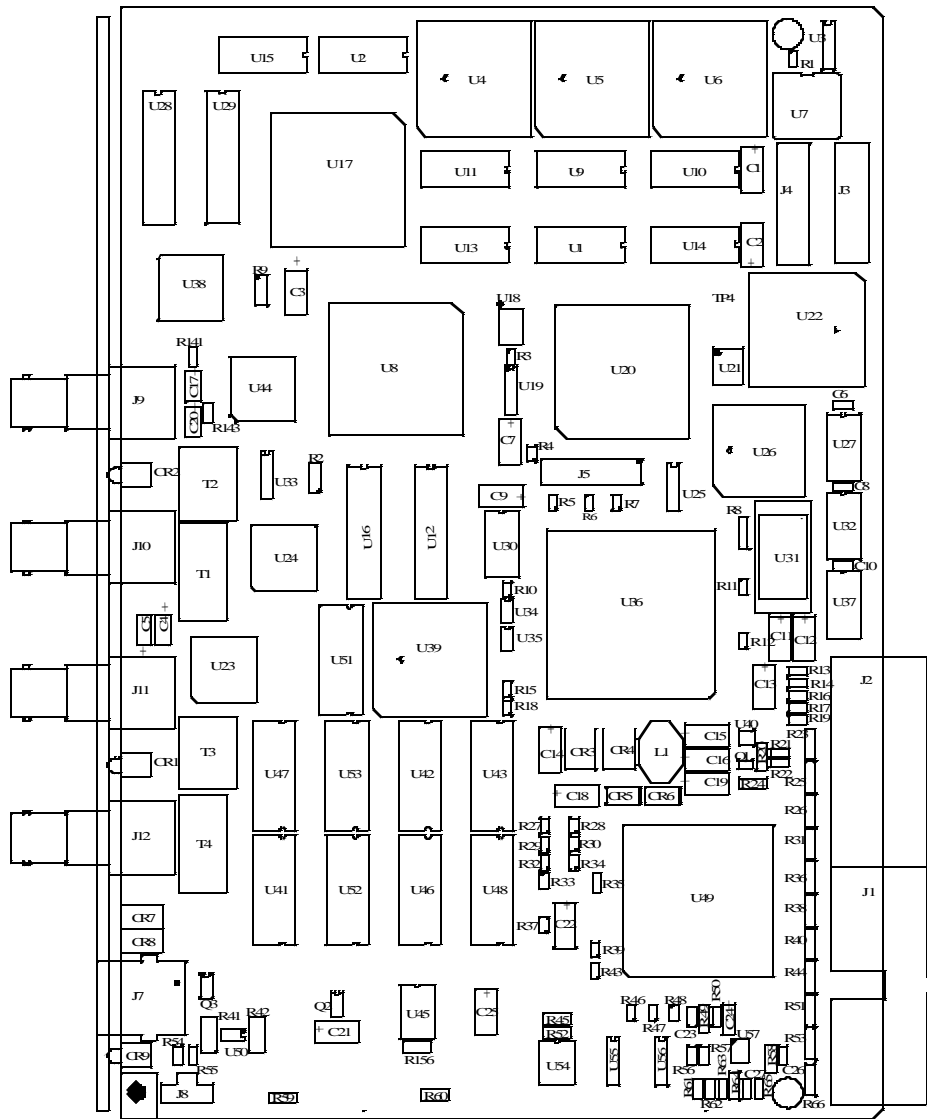


Figure 1-2. Physical Configuration

Figure 1-2 is a physical diagram of the CPCI-817 Adapter, showing the location designators of jumpers, connectors, and ICs. Refer to this figure when component locations are referenced in the manual text.

1.7 REFERENCE MANUALS

- | | |
|--|---|
| <p>MPC8240 Integrated Processor User's Manual
Order Number MPC8240UM/D Rev. 0
Motorola Literature Distribution
P.O. Box 5405
Denver, CO 80217
(800) 441-2447</p> | <p>LM75 Digital Temperature Sensor and Thermal Watchdog
National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
(800) 272-9959</p> |
| <p>PowerPC Microprocessor Family:
The Programming Environments for
32-bit Microprocessors, Rev. 1
Order Number MPCFPE32B/AD
Motorola Literature Distribution
P.O. Box 5405
Denver, CO 80217
(800) 441-2447</p> | <p><i>CompactPCI</i> OS Specification PICMG 2.0 R3.0
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax</p> |
| <p>TL16C550C UART
Texas Instruments
http://www.ti.com/sc/docs/general/dsmenu.htm</p> | <p>PCI Local BIOS Specification, Revision 2.2
PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97214
(800) 433-5177 (U.S.)
(503) 693-6232 (International)
(503) 693-8344 (Fax)</p> |
| <p>PCI-9080
PLX Technology, Inc.
390 Potrero Avenue
Sunnyvale, CA 94086
(800) 759-3735
(408) 774-2169 Fax
http://www.plxtech.com</p> | <p>I₂O Specification, Revision 1.0
I₂O Special Interest Group
(415) 750-8352
http://www.i2osig.org</p> |
| <p>Local ATM SAR Chip User's Manual
(uPD 98401)
NEC Electronics, Inc.
475 Ellis Street
P.O. Box 7241
Mountain View, CA 94039</p> | <p><i>CompactPCI</i> OS Hot Swap Specification, PICMG 2.1, R1.0
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax</p> |
| <p>E1 Framer/Transceiver
(E1XC, PM6341A)
Saturn User Network Interface
(S/UNI-PDH, PM7345)
PMC-Sierra, Inc.
8501 Commerce Court
Burnaby, BC Canada V5A 4N3
(604) 668-7300</p> | |

2.1 MPC8240 PROCESSOR

The MPC8240 contains a PowerPC 603e core processor. The core is configured to run at 250 MHz. This RISC processor utilizes a superscalar architecture that can issue and retire as many as three instructions per clock. The core features independent 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs).

2.2 BYTE ORDERING

The CPCI-817 is designed to run in big endian mode. The byte ordering determines how the core accesses local memory and the PCI bus. Big endian stores the most significant byte in the lowest address.

2.3 RESET VECTOR

The 8-bit wide Flash ROM is located in the address range FFE0 0000h through FFFF FFFFh. See Figure 2-1, the CPCI-817 memory map. The MPC8240 reset vector is located at address FFF0 0100h. This reset vector location, which contains a branch to the rest of the boot code, is essentially in the middle of the ROM device. This positioning results in a break up of continuous memory space and approximately 50% reduction in usable space for boot code. To better utilize this device, the CPCI-817 re-maps the reset vector to FFE0 0100h by inverting memory address 20 (A20) for the first two processor accesses to memory. These accesses are an absolute jump instruction to the beginning of boot code. After this jump, A20 functions normally. Utilizing this method, the majority of the 2 Mbyte Flash ROM can be used.

2.4 POWERPC MPC603E CORE CACHE, BUFFERS, ARRAYS

The processor core provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data, and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set associative, data and instruction lookaside buffers (TLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The processor also supports block address translation (BAT) arrays of four entries each.

As an added feature to the MPC603e core, the MPC8240 can lock the contents of one to three ways in the instruction and data cache (or the entire cache).

2.5 MEMORY MAP

Figure 2-1 shows the CPCI-817 memory map.

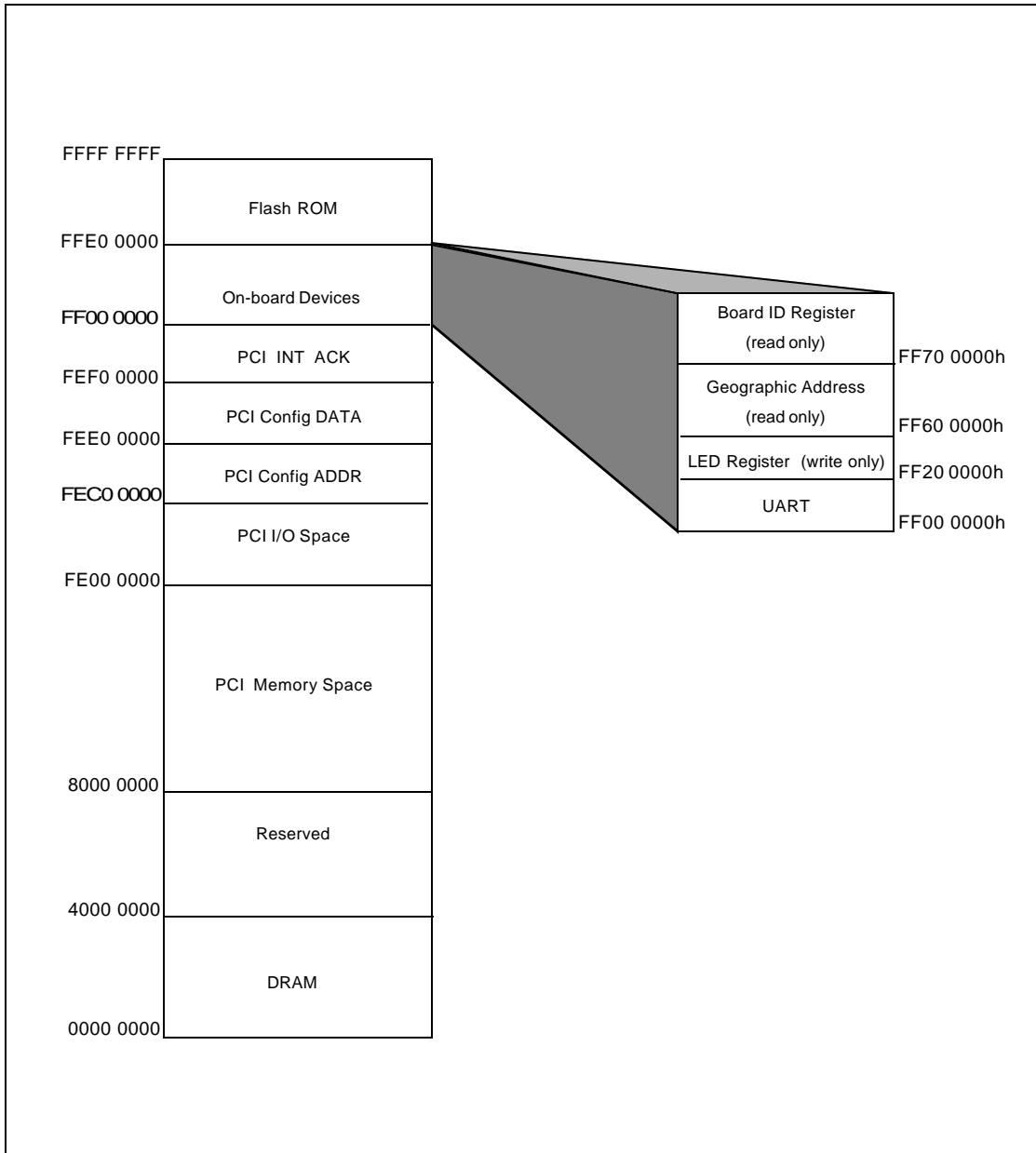


Figure 2-1. CPCI-817 Memory Map

2.6 INTERRUPTS

The CPCI-817 interrupt scheme is based upon the MPC8240 processor’s embedded programmable interrupt controller (EPIC). The EPIC unit is set to serial interrupt mode. Serial interrupt mode allows for a maximum of 16 external interrupts. Table 2-1 shows the assignment of devices to serial interrupts on the CPCI-817, all the interrupts are level sensitive.

The EPIC interface also contains several internal interrupt sources. These include the four global timers, the two DMA channels, the I²C bus, and the Message Unit.

In addition to the EPIC interface, errors detected by the MPC8240 are reported to the processor core by asserting an internal machine check signal. Many of the errors detected in the MPC8240 cause exceptions to be taken by the processor core. The error reporting is provided for three of the primary interfaces, processor core interface, memory interface, and the PCI interface.

The ATM-SARs, E1XCs and SUNI_PDHs generate interrupts. The SUNI-PDHs and E1XCs interrupt via the ATM-SARs. Thus there are only two interrupts required SAR1_INT and SAR2_INT. If the SUNI_PDH or E1XC is the interrupt source, the ATM-SARs will interrupt the host and will have a bit set in its status register, indicating that the SUNI-PDH or E1XC was the interrupt source.

Table 2-1. Serial Interrupt Assignment

INTERRUPT	INTERRUPT SOURCE	POLARITY
0	MIC_INTB	0
1	MIC_INTA	0
2	SAR1_INT	0
3	SAR2_INT	0
4	UART	1
5	Temperature (LM75s)	0
6	LSERR (PCI9080)	0
7	SINT A (21554)	0
8	MIC_INTD	0
9	MIC_INTC	0
10	Not Used	X
11	Not Used	X
12	Not Used	X
13	Not Used	X
14	Not Used	X
15	Not Used	X

2.6.1 MPC8240 Interrupt Registers

The MPC8240 processor has several different EPIC register maps to facilitate the handling of interrupts which are briefly mentioned below. These registers occupy a 256Kbyte range of the embedded utilities memory block (EUMB) and can be read and written by software. Please refer to the Motorola MPC8240 User’s Manual for more details.

Global EPIC Registers	Provides programming control for resetting, configuration and initialization of the external interrupts. Additionally, a vector register is provided to be returned to the processor during an interrupt acknowledge cycle for a spurious vector.
Global Timer Registers	Each of the four global timers have four individual configuration registers. The registers are the Current Count register, the Base Count register, the Vector/Priority register, and the Destination register.
Interrupt Source Configuration	This group of registers are made up of the vector/priority and destination registers for the serial and internal interrupt sources. This includes the masking, polarity, and sense.
Processor-Related Registers	This group describes the processor-related EPIC registers. They are made up of the Current Task Priority register, the Interrupt Acknowledge register, and the End of Interrupt register.

2.6.2 Error Handling and Exceptions

Errors detected by the MPC8240 are reported to the processor core by asserting an internal machine check signal (mcp#). The MPC8240 detects illegal transfer types from the processor, illegal Flash write transactions, PCI address and data parity errors, accesses to memory addresses out of the range of physical memory, memory parity errors, memory refresh overflow errors, ECC errors, PCI master-abort cycles, and PCI received target-abort errors. Table 2-2 describes the relative priorities and recoverability of externally-generated errors and exceptions.

Table 2-2. Error Priorities

Priority	Exception	Cause
0	Hard reset	Power-on reset, CompactPCI chassis reset switch or via JTAG controller
1	Machine check	Processor transaction error or Flash error
2	Machine check	PCI address parity error or PCI data parity error when the CPCI-817 is acting as the PCI target
3	Machine check	Memory select error, memory refresh overflow, or ECC error
4	Machine check	PCI address parity error or PCI data parity error when the CPCI-817 is acting as the PCI master, PCI master-abort, or received PCI target-abort

3.1 SDRAM

The CPCI-817 is equipped with 64 Mbytes of ECC SDRAM mounted on the card. The memory is made up of nine, 64Mbit (8M x 8) devices in an 8M by 72-bit configuration.

The memory controller unit (MCU) of the CPCI-817 supports SDRAM burst lengths of four. A burst length of four enables seamless read/write bursting of long data streams as long as the MCU does not cross the page boundary. Page boundaries are naturally aligned 2 Kbyte blocks. 72-bit SDRAM with ECC running at 100MHz allows a maximum throughput of 800 Mbytes per second. The MCU keeps four pages open simultaneously. Simultaneously open pages allow for greater performance for sequential access, distributed across multiple internal bus transactions.

3.2 CONTROL MEMORY, E1XC & SUNI-PDH REGISTERS

The CPCI-817's SRAM is control memory used exclusively by the ATM-SARs. The control memory can be accessed via the ATM-SARs using an INDIRECT_ACCESS command. Parity generation and checks are not performed on the control memory. As shown in the figure, the SUNI-PDH and E1XC processor interfaces are also attached to the control memory bus. The SUNI-PDH and E1XC registers are accessed via the ATM-SARs using an INDIRECT_ACCESS command.

3.3 FLASH ROM

The CPCI-817 provides 2 Mbytes of sector-programmable Flash ROM for non-volatile code storage. The Flash ROM is located in local memory space at address FFE0 0000h through FFFF FFFFh. The mapping ensures that, after a reset, the MPC8240 processor can execute the hard reset exception handler located at FFF0 0100h.

3.4 CONSOLE SERIAL PORT

A single console serial port with an RS-232 line interface has been included on the CPCI-817. The port is connected to a RJ-11 style phone jack on the adapter, and can be connected to a host system using the included phone jack to DB-25 cable (Cyclone P/N 530-2002). The pinout of the console connector is as shown in Table 3-1.

Table 3-1. Console Port Connector

Pin	Signal	Description
1		Not Used
2	GND	Ground
3	TXD	Transmit Data
4	RXD	Receive Data
5		Not Used
6		Not Used

K Note

Pin 1 is the contact to the extreme left look in the console port opening, with the tab notch facing down.

The serial port is based on a 16C550 UART clocked at 1.843 MHz. The device may be programmed to use this clock with the internal baud rate counters. The serial port is capable of operating at speeds from 300 to 115200 BPS, and can be operated in interrupt-driven or polled mode. The 16C550 register set is shown in Table 3-2. For a detailed description of the registers and device operation refer to the 16C550 databook.

Table 3-2. UART Register Addresses

Address	Read Register	Write Register
FF00 0000H	Receive Holding Register	Transmit Holding Register
FF00 0008H	Unused	Interrupt Enable Register
FF00 0010H	Interrupt Status Register	FIFO Control Register
FF00 0018H	Unused	Line Control Register
FF00 0020H	Unused	Modem Control Register
FF00 0028H	Line Status Register	Unused
FF00 0030H	Modem Status Register	Unused
FF00 0038H	Scratchpad Register	Scratchpad Register

3.5 COUNTER/TIMERS

The MPC8240 processor is equipped with four 31-bit on-chip counter/timers which count at 1/8 the frequency of the SDRAM_CLK signal or 12.5MHz. Users should refer to the Processor User's Manual for the functionality and programming of the counters. The timers can be individually programmed to generate interrupts to the processor when they count down to zero. Two of the timers, timer2 and timer3, can be set up to automatically start periodic DMA operations for DMA channels 0 and 1, respectively, without using the processor interrupt mechanism.

3.6 LEDS

The CPCI-817 has six green LEDs and one blue LED. The four green LEDs labeled IOP, ACT, STAT0, and STAT1 are software driven and are controlled by a write-only register which is located at address FF20 0000H. The LED Register bitmap is shown in Figure 3-1. Two green LEDs labelled LINK0 and LINK1 are under ATM hardware control and indicate a valid E1 link once the SUNI-PDH devices have been initialized by software.

The blue LED is used for Hot Swap operations. Refer to section 3.14.1 for additional information.

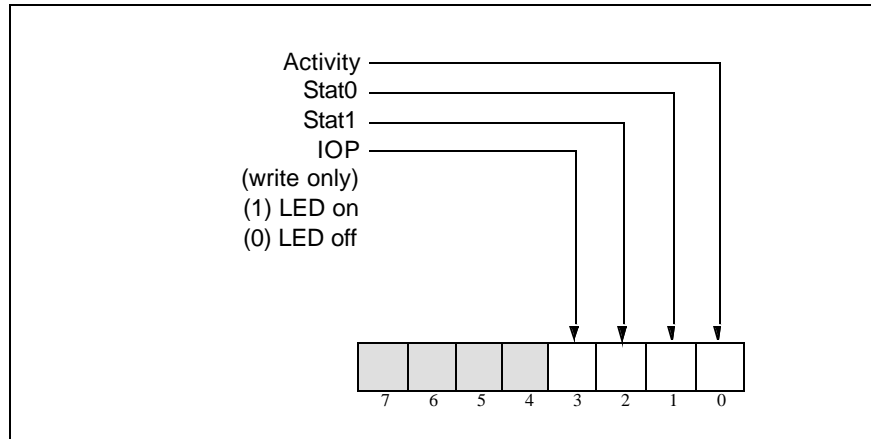


Figure 3-1. LED Register Bitmap, FF20 0000H

3.7 PCI INTERFACE

The CPCI-817 contains a primary 64-bit PCI bus and a secondary 32-bit PCI bus. Both buses are clocked at 33 MHz. The primary PCI bus interfaces the 64-bit CompactPCI bus to the 21554 PCI-to-PCI bridge. The secondary side of the 21554 interfaces a 32-bit PCI bus to the MPC8240 and the PCI9080 bridge, which interfaces the two ATM SARs.

3.7.1 Primary PCI Arbitration

The primary PCI bus arbitration is provided by the host of the CompactPCI system.

3.7.2 Secondary PCI Arbitration

Secondary bus arbitration logic between the MPC8240 processor, the 21554 bridge and the PCI9080 bridge, is contained within the MPC8240. The bus arbitration unit allows fairness as well as a priority mechanism. A two-level round-robin scheme is used, in which each device can be programmed within a pool of high- or low-priority arbitration. One member of the low-priority pool is promoted to the high-priority pool. As soon as it is granted the bus it returns to the low-priority pool.

3.8 DMA CHANNELS

The MPC8240 processor features two DMA channels. Data movement occurs on the PCI and/or memory bus. Each channel has a 64-byte queue to facilitate the gathering and sending of data. Both the local processor and PCI masters can initiate a DMA transfer. Some of the features of the MPC8240 DMA unit include: misaligned transfer capability, scatter gather DMA chaining and direct DMA modes, and interrupt on completed segment, chain, and error. Figure 3-2 provides a block diagram of the MPC8240 DMA unit.

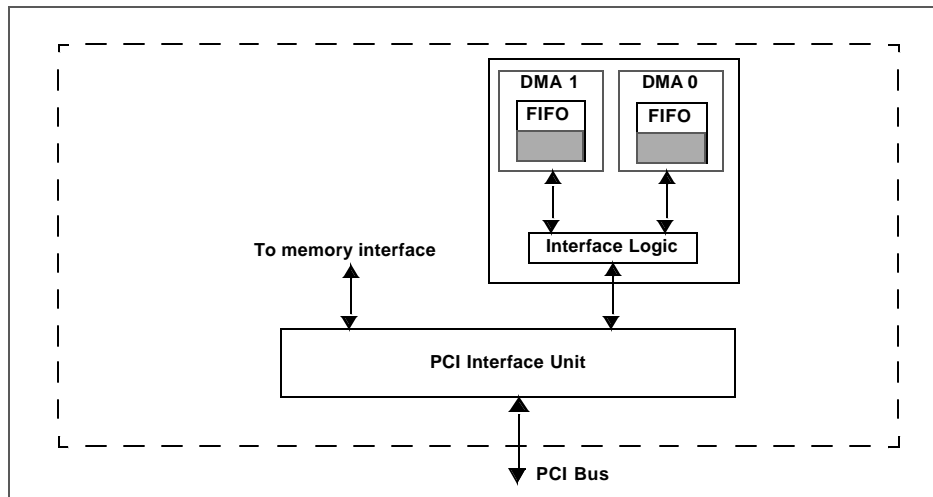


Figure 3-2. MPC8240 Processor DMA Controller

3.9 MESSAGE UNIT

The MPC8240 provides a message unit (MU) to facilitate communications between the host processor and peripheral processors. The MPC8240's MU can operate with generic messages and doorbell registers, and also implements an I₂O compliant interface.

The Intelligent Input Output (I₂O) specification allows architecture-independent I/O subsystems to communicate with an OS through an abstraction layer. The specification is centered around a message-passing scheme. An I₂O-compliant peripheral (IOP) is comprised of memory, processor, and input/output devices. The IOP dedicates a certain space in its local memory to hold inbound (from the remote processor) and outbound (to the remote processor) messages. The space is managed as memory-mapped FIFOs with pointers to this memory maintained through the MPC8240 I₂O registers. Please refer to the MPC8240 User's Manual for I₂O register descriptions, FIFO descriptions and an I₂O message queue example.

3.10 JTAG/COP SUPPORT

The MPC8240 provides a Joint Test Action Group (JTAG) interface. Additionally, the JTAG interface is also used for accessing the common on-chip processor (COP) function of PowerPC processors. The COP function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor. The 16 pin COP header (sample part is Samtec # HTSW-108-07-S-S) is located at J5. The COP header adds many benefits including breakpoints, watchpoints, register and memory examination/modification and other standard debugger features. The COP header definition is shown in Table 3-3. The location of pin 1 on the header is indicated by the "dot" on the top right corner of the J5 designer in the silk screen, as in Figure 3-3.

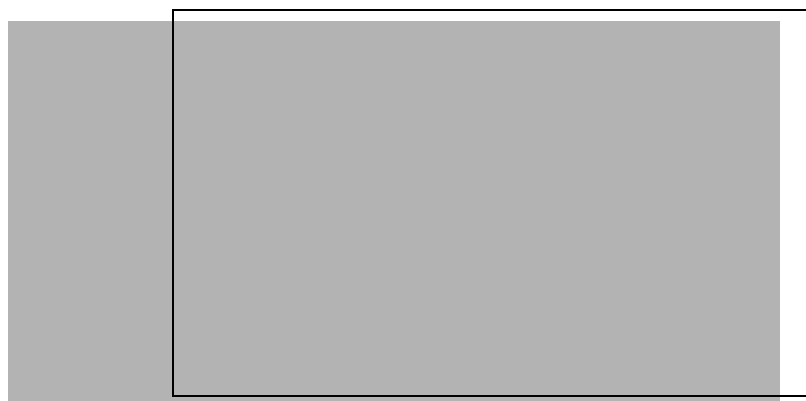


Figure 3-3. JTAG/COP Header Orientation

Table 3-3. JTAG/COP PIN ASSIGNMENT

Signal	Pin	Pin	Signal
TDO	1	2	QACK#
TDI	3	4	TRST#
Pull-up to +3V	5	6	+3V
TCK	7	8	CHKSTOPIN#
TMS	9	10	N/C
SRESET#	11	12	GND
COP_RESET#	13	14	N/C
Pull-Up to +3V	15	16	GND

3.11 GEOGRAPHIC ADDRESSING

CompactPCI backplanes that support 64-bit connector pin assignments are required to provide a unique differentiation based upon which physical slot the board has been inserted. The CPCI-817 makes this definition available to the software. The definition for GA[4:0] is shown in Figure 3-4.

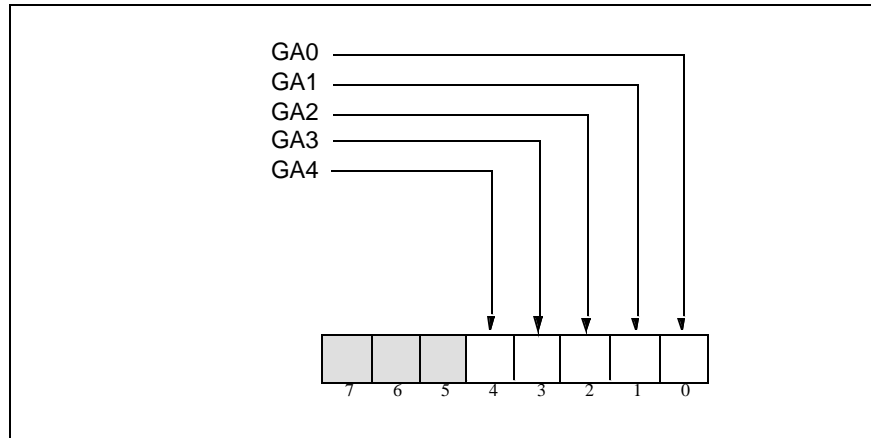


Figure 3-4. Geographic Addressing Register, FF60 0000H.

3.12 I²C BUS

The CPCI-817 has two temperature sensors attached to the Inter-Integrated Circuit (I²C) bus interface of the MPC8240 processor. The I²C addresses of the devices are shown in Table 3-4.

Table 3-4. I²C Device Addresses

Designator	Device	Function	Address
U34	LM75	Temperature Sensor	1001000
U35	LM75	Temperature Sensor	1001001

3.12.1 Temperature Sensors

The LM75 temperature sensors have overtemperature trip points that will trigger an interrupt when crossed. The sensors are placed on the board at U34 and U35, and share serial interrupt #5. The sensors should be placed in the interrupt mode by startup code. The sensors can be read for a temperature reading at any time; reading after an interrupt clears the interrupt. The sensor will not interrupt again until the temperature has dropped below the hysteresis setting. Consult the LM75 data sheet for more details on programming the temperature sensors.

3.13 HOT SWAP

The CPCI-817 is a PICMG 2.1 compliant Hot Swap board. The CPCI-817 is a “Full Hot Swap” board, with both Hardware and Software Connection control. The CPCI-817 can be used on all platform types; Non-Hot Swap platform for a conventional system, Hot Swap platform for a Full Hot Swap system and on High Availability platform for a High Availability system. See the Hot Swap specification for further explanation of platform, board and system types.

3.13.1 Hot Swap Extraction Process

Removal of the CPCI-817 in a Full Hot Swap or High Availability system is the same. The operator first only opens the ejector handles of the board. A switch on the CPCI-817 signals to the system that it is to be extracted. In response, the system will illuminate the blue Hot Swap LED when extraction is permitted.

3.13.2 Hot Swap Insertion Process

Insertion of the CPCI-817 is the same in any Hot Swap system. The operator slides the CPCI-817 into the desired slot and latches the handles.

3.14 BNC CONNECTOR

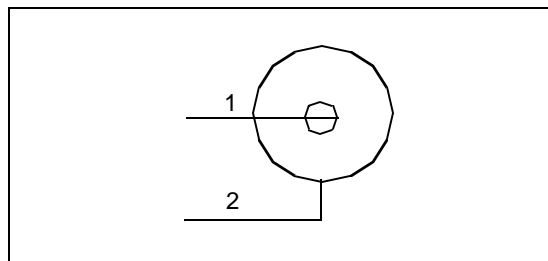


Figure 3-5. BNC-RA-75 Ohm

3.14.1 E1 CONNECTOR

The CPCI-817 uses 75 ohms BNC connectors for the E1 line interface. Table 3.5 lists the pin connections and the signal description.

Table 3-5. E1 Connector

E1 Ports	PIN		SIGNAL	DESCRIPTION
Port 0 'RCV'	J12	2	R0XR0	Receive Ring 0
	J12	1	R0XT0	Receive Tip 0
Port 0 'XMT'	J11	2	T0XR0	Transmit Ring 0
	J11	1	T0XT0	Transmit Tip 0
Port 1 'RCV'	J10	2	R1XR1	Receive Ring 1
	J10	1	R1XT1	Receive Tip 1
Port 1 'XMT'	J9	2	T1XR1	Transmit Ring 1
	J9	1	T1XT1	Receive Tip 1

3.15 BOARD ID REGISTER

The Board ID Register is a read-only register that can be used to differentiate between the CPCI-817 and other Cyclone Microsystems MPC8240-based CompactPCI cards. It is located at address FF70 0000h on all such cards, with each card returning a unique ID value. Figure 3-5 shows the board ID for the CPCI-817.

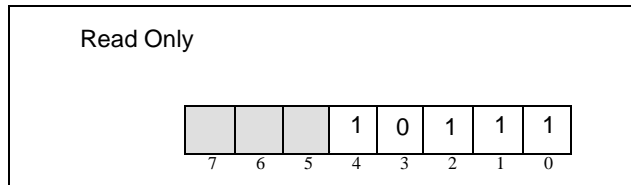


Figure 3-6. Board Identification Registers, FF70 0000h

CHAPTER 4

ATM PROGRAMMING INFORMATION

4.1 INTRODUCTION

The Control Memory, the E1XC registers and the SUNI-PDH registers are accessed through the ATM-SAR. The Control Memory, the E1XC and the SUNI-PDH are accessed using the COMMAND REGISTER (CMR), COMMAND EXTENSION REGISTER (CER) and the INDIRECT ACCESS COMMAND of the ATM-SAR.

The INDIRECT ACCESS COMMAND has a two bit field that indicates the target of the access; Control Memory (00), ATM-SAR registers (01), PHY device (11). The PHY device target should be used to access both the E1XC registers and the SUNI-PDH registers. The E1XC registers have an offset of 100h; the SUNI-PDH registers reside at 000h through 074h.

Table 4-1. Secondary Address Map for ATM-SAR Registers

ATM-SAR Registers	ATM-SAR Offset
GMR	00h
GSR	04h
IMR	08h
RQU	0ch
RQA	10h
ADDR	14h
VER	18h
SWR	1ch
CMR	20h
CMR_L	24h
CER	28h
CER_L	2ch
MSH0	40h
MSH1	44h
MSH2	48h
MSH3	4ch
MSL0	50h
MSL1	54h
MSL2	58h
MSL3	5ch
MBA0	60h
MBA1	64h
MBA2	68h
MBA3	6chh
MTA0	70h

MTA1	74h
MTA2	78h
MTA3	7ch
MWA0	80h
MWA1	84h
MWA2	88
MWA3	8ch

4.2 DEVICE REGISTERS

The ATM-SAR, SUNI-PDH and E1XC are very flexible devices, and therefore have many registers that can be setup to customize device operation. The following three sections identify register settings.

4.2.1 ATM-SAR Mode Registers

The ATM-SAR device has a mode register that configures the device for various modes of operation. Almost all of the bit settings for the mode registers have already been determined and fixed by the hardware design.

Table 4-2 shows the bit settings for the ATM-SAR mode register. Entries of “D” under “Val” indicate that the entry is a don’t care; the bit can be set to zero or one. An “S” under “Val” means that the user can set this for his application. Consult the ATM-SAR Chipset User’s Manual for more information.

Table 4-2. ATM-SAR General Mode Register

Bit#	Value	Name	Status/Function
0	S	RE	Receiver Enable/Disable
1	S	SE	Transmitter Enable/Disable
2	S	DR	Receive Drop Mode
3	0	BPE	Bus Parity Disabled
4	D	PC	Bus Parity Disabled
5	D	PM	Bus Parity Disabled
6	0	BO	Little endian Byte Ordering
7	0	AD	Burst Size Determined from Address
8	1	SZ	2 Word Bursts Enabled
9	1	SZ	4 Word Bursts Enabled
10	1	SZ	8 Word Bursts enabled
11	1	SZ	16 Word Bursts Enabled
12	0	RA	Read RDY Mode Normal
13	0	WA	Write RDY Mode Normal
14	S	LP	Normal/Loopback Mode
15	0	CPE	Control Memory Parity Disabled
16	1	TBE	12-word burst enable

17-24	0	----	Reserved
25	0	----	Reserved
26	0	UDC	Utopia mode
27	0	PSM	Receive Report Mode
28	0	1CM	Idle cell mode
29	0	----	Reserved
30	1	SLM	Sets Registers to Word Boundaries
31	1	----	Set to 1 for Proper Operation

4.2.2 SUNI-PDH REGISTERS

The registers listed in Table 4-3 have been modified from their power-up, reset default values. In general the SUNI-PDH is setup for direct cell mapping, HEC cell delineation and no payload scrambling as required by the ATM Forum DS1 Physical Layer Specification. All interrupts are disabled and loopback modes are not enabled. Also see the SUNI-PDH manual section "Basic Operating Modes."

Table 4-3. SUNI-PDH Non-Default Register Settings

ADDR	DATA	Register name and Description
000h	08h	SUNI_PDH Configuration Setting the FRMRBPP bit (bit3) bypasses the DS3/E3 framer.
028h	C0h	SPLR Configuration Setting the FROM [1:0] bits (bits 7,6) to [1,1] selects E1 framing format and clearing the PLCPEN bit (bit 2) disables the PLCP framing function of the SMDS PLCP Layer Receiver Block.
02Ch	C0h	SPLT Configuration Setting the FROM [1:0] bits (bits 7,6) to [1,1] selects E1 framing format and clearing the PLCPEN bit (bit 2) disables the PLCP framing function of the SMDS PLCP Layer Transmitter block.
040h	28h	RXCP Control Setting the HCSADD bit (bit 5) enables the addition of the coset polynomial to the received HCS octet before comparison with the calculated result. Clearing the DSCR bit (bit 3) disables the payload descrambling function. Setting the BLOCK bit (bit3) blocks Idle/ Unassigned cells from the receiver FIFO.
041h	01h	RXCP Framing Control Setting the DELIN bit (bit0) enables the ATM cell. Delineator (ATMF) Block. That is, HEC based cell delineation is enabled.
046h	01h	RXCP Idle/Unassigned Cell Pattern:H4 octet Setting the receive idle/ unassigned cell pattern for the H4 octet to 01h causes idle cells to be filtered and clearing to 00h causes unassigned cells to be filtered, if the mask pattern for the H4 octet is configuring to look at all bits in the octet. See the setting of the RXCP Idle/Unassigned Cell Mask:H4 octet (ADDR=04Ah).

047h	FFh	RXCP Idle/Unassigned Cell Mask: H1 octet
048h	FFh	RXCP Idle/Unassigned Cell mask: H2 octet
049h	FFh	RXCP Idle/Unassigned cell Mask: H3 octet Setting the receive idle/unassigned cell mask for the H1, H2 and H3 octets to FFh causes all bits in all three octets to be compared with their corresponding RXCP Idle/Unassigned Cell Patterns.
04h	FEh	RXCP Idle/Uassigned Cell Mask:H4 octet Setting the receive idle/unassigned cell mask for the octet to FEh cause all bits except bit 0 of the H4 octet to be compared with their corresponding RXCP Idle/Uassigned Cell pattern. With this setting, both idle cells(H4=01h) and unassigned cells (H4=00h) get filtered from the receive FIFO.
04F	FFh	RXCP User Idle Frame Filter
050	FFh	RXCP User Idle Frame Filter
051	FFh	RXCP User Idle Frame Filter
052	FFh	RXCP User Idle Frame Filter
058H	A0h	TXCP Control Setting the HCSADD bit (bit5) enables the addition of the coset polynomial to the HCS octet before transmission. Clearing the SCR bit (bit 2) disables the payload scrambling function. Setting the HCSINS bit (bit7) forces the calculated HCS to overwrite the HCS octet, that is the SUNI_PDH generates and inserts the HCS. Clearing the FIFODP [1:0] bits (bits 4,3) sets the transmit FIFO depth to 4 cells.
059h	01h	TXCP Interrupt Enable/Status Setting the TFULL4 bit(bit4) sets the TFIFOFB/TCA pin to behave as an “almost full” indication. This was found to work best with the ATM_SAR.
05Dh	01h	TXCP Idle/Unassigned Cell Pattern: H4 octet Setting the transmit idle/unassigned cell pattern for the H4 octet to 01h Causes idle cells to be generated. Clearing it to 00h causes unassigned cells to be generated.
05Eh	52h	TXCP Idle/Uassigned Cell Pattern: H5 octet Setting the transmit idle/unassigned cell pattern for the H5 octet to 52h is the correct HCS for idle cells. Setting the H5 octet to 55h is the correct HCS for unassigned cells.
05Fh	6Ah	TXCP Idle/Unassigned Cell Payload Setting the transmit idle/unassigned cell payload to 6Ah is the correct value for idle or unassigned cells.

4.2.3 E1XC Registers

The registers listed in the Table 4-4 have been modified from their power-up, reset default values. The E1XC is setup for 24 frame Extended Superframe Format (ESF) and Bipolar 8 Zero Substitution (B8ZS) line coding as required by the ATM Forum DS1 Physical Layer Specification. All interrupts are disabled. Loopback modes are not enabled. Also see the E1XC manual section “Configuring the E1XC from Reset.”

Table 4-4. E1XC Non-Default Register Settings

ADDR	DATA	Register Name and Description
100h	20h	E1XC Receive Options Setting the ELSTBYP bit(bit5) bypasses the elastic store block of the E1XC, keeps the data synchronized to the recovered clock (RCLKO) and eliminates the need for a BRCLK.
101h	10h	E1XC Receive Backplane Options Overhead output mode.
103h	40h	E1XC Receive DS1 Interface Configuration Setting the SDOEN bit (bit 6) forces the multifunction (input/output) pins SDP/RDP/RDD and SDN. RDN/RLCV to outputs, eliminating the need for support of the multifunction pins as digital inputs.
105h	00h	E1XC Transmit Backplane Options Single rail mode
114h	64h	XPLS Line Length Configuration ILS [2:0] bits (bits 2, 1, 0) set for G.703 120 ohm line. See the E1XC manual for more information.
120h	00h	FRMR Configuration Standard Framing Format. See the E1XC manual for more information.
130h	02h	TPSC Configuration Set the IND bit (bit 1) for proper operation.
140h	02h	SIGX Block Configuration Indirect Access
144h	60h	Tran Block Configuration CAS enabled
146h	FFh	Tran Block International Control Default international bits.
147h	FFh	Tran Block Extra Bits Extra bits not used.
15ch	01h	RSLC Block Configuration 50% slicing threshold

4.3 SOFTWARE RESET

All six VLSI devices (2 ATM-SARs, 2 SUNI-PDHs and 2 E1XCs) can be reset by software. The actions required to reset the devices follow and the equivalent of asserting their respective reset pins.

4.3.1 ATM-SARs Software Reset

The ATM-SAR is reset when any value is written to the software reset register at offset 0000 001Ch.

4.3.2 SUNI-PDHs Software Reset

The SUNI_PDH is reset when 0x08h (or any other value that sets bit 7 to a one) is written to the Identification and Master Reset Register at offset 0x04h. The SUNI-PDH will remain reset until a 0x00h (or any other value that clears bit 7 to a zero) is written to offset 0x04h.

4.4 LOOPBACK

The ATM-SAR, SUNI-PDH, and E1XC each has one loopback path.

Loopback paths within the ATM-SARs is performed by setting the LP bit (bit 14) of the ATM-SAR's General Mode Register. A multiplexer internal to the ATM-SAR allows data to traverse the entire transmit and receive data paths of the ATM-SAR. See the ATM-SAR User's Manual for more reference.

The diagnostic loopback of the SUNI_PDH is obtained by setting the DLB bit (bit 2) of the SUNI-PDH's Configuration Register (0x00h). Like the ATM-SAR loopback, the diagnostic loopback connects the transmit data to the receive data, allowing data to traverse the transmit and receive data paths of the SUNI-PDH.

Like the loopbacks for the ATM-SAR and SUNI-PDH, the two loopback modes available in the E1XC connect transmit data to receive data. The diagnostics digital loopback is enabled by setting the DDLB bit (bit 2) of the E1XC Master Diagnostics register (0x10Ah). This mode loops transmit data to receive data, but does not include the analog drivers of the E1XC. The diagnostic metallic loopback is enabled by setting the DMLB bit (bit 3) of the E1XC Master Diagnostics register (0x10Ah). This mode loops transmit data to receive data just after the analog drivers of the E1XC.

4.5 CLOCKING OPTIONS

In normal operation, the transmit clock is derived from the receive data. Loop timing is enabled by setting the LOOPT bit (bit 4) of the SUNI-PDH Configuration Register (0x000h).