COMPACTPCI-815
SYSTEM CONTROLLER
USER'S MANUAL

Revision 1.0, May 2001

Cyclone P/N 800-0815

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1
GENERAL INTRODUCTION

1.1 INTRODUCTION

The CPCI-815 is a high-performance CompactPCI peripheral board featuring two Ethernet Controllers and PMC Module. A block diagram is shown in Figure 1-1.

The board is based on the MPC8240 PowerPC™ integrated processor. The MPC8240 has a processor core based on the PowerPC603e™ low-power microprocessor, and also performs many peripheral functions on chip. The peripheral logic integrates a PCI bridge, memory controller, DMA controller, interrupt controller, I_2O controller, and an I^2C controller.

Software development tools for PowerPC processors are available from a variety of vendors, and Board Support Packages (BSPs) for the PSOS operating system is available from Cyclone.

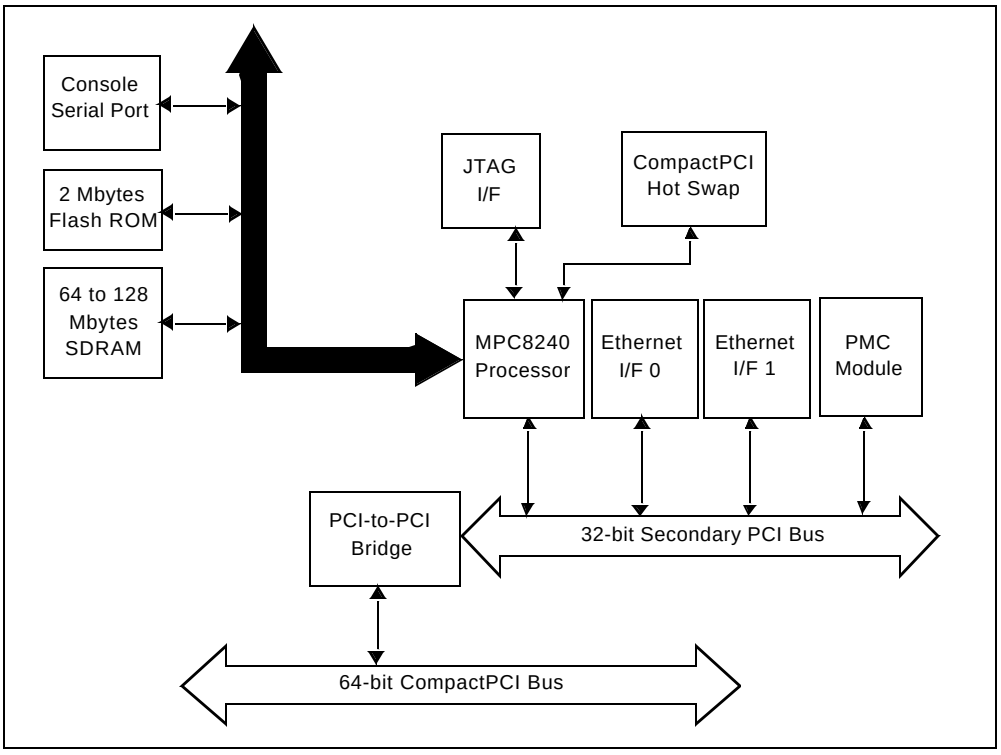

Figure 1-1. CPCI-815 Block Diagram

1.2 FEATURES

- MPC8240 Processor — The microprocessor is Motorola's integrated MPC8240 PowerPC. The device integrates a Motorola 32-bit superscalar PowerPC 603e core, running at 250 MHz internally, and a Peripheral Components Interconnect (PCI). The core boasts a 16 Kbyte instruction cache, a 16 Kbyte data cache and floating-point support. Memory can be accessed through the memory controller to the core processor or from the PCI bus.
- 21554 PCI-to-PCI Bridge — The 21554 is a "non-transparent" PCI-to-PCI bridge with a 64-bit primary bus interface and a 64-bit secondary interface. A non-transparent bridge allows the local processor to configure and control the local subsystem. The 21554 primary bus interfaces with the 64-bit CompactPCI bus and the secondary bus interfaces with the 32-bit PCI bus of the MPC8240.
- SDRAM — 64 MBytes of ECC SDRAM is standard on the CPCI-815.
- PMC Module — PCI Mezzanine cards use the logical and electrical layers of the PCI specification for the local bus. I/O can be via the front bezel and/or through the connector to the host for backplane I/O. 32-bit PCI bus requires two 64 pin connectors Pn1/Jn1 and Pn2/Jn2.
- *CompactPCI* Interface — The CPCI-815 meets the PICMG 2.0 R3.0 Specification for peripheral slot adapters. The PCI bus runs at 33MHz.
- Flash ROM — 2 Mbytes of in-circuit sector-programmable Flash ROM.
- 82559ER Ethernet Controllers — The 82559 provides a higher level of integration, enhanced features, reduced power consumption, and small footprint (15mm x 15mm). THe 82559 has been optimized to accelerate the integration of LAN into desktop, server, PC cards, docking stations and mobile platforms.
- Console Serial Port — An RS-232 serial port is provided for a console terminal or workstation connection. The serial port supports up to 115 Kbps and uses a phone jack to DB25 cable supplied with the CPCI-815 board.
- Hot Swap — The CPCI-815 is a full Hot Swap board, compliant with PICMG 2.1 R2.0.
- Timers — Four 31-bit timers are available to generate interrupts.
- DMA Controller — The MPC8240 supports 2 separate DMA channels for high throughput data transfers between PCI bus agents and the local SDRAM memory.
- I_2O Messaging — The CPCI-815 supports the I_2O specification for interprocessor communication.

1.3 OVERVIEW

The CPCI-815 is 6U CompactPCI System peripheral board with two Ethernet Controllers and PMC Module. The CPCI-815 has two PCI buses, a Primary and Secondary. The Primary PCI bus is the CompactPCI bus. The Secondary PCI bus is a local bus that supports the MPC8240. The CPCI-815 uses an Intel 21554 Embedded PCI-to-PCI Bridge to bridge between the Primary Compact PCI bus and the Secondary local PCI bus. The device complies with the PCI Local Bus Specification (revision 2.1), provides concurrent bus operation, allows buffering for both read and write transactions, and provides support for Hot Swap operation.

The Primary PCI interface is 64-bit data, but will operate correctly when the CPCI-815 is plugged into a 32-bit CompactPCI slot. Although the Secondary PCI bus of the 21554 is 64-bit data, the local bus of the CPCI-815 is 32-bit (the MPC8240). The data path to memory of the CPCI-815 is 64-bit. The memory controller resides on the MPC8240.

The Flash ROM on the CPCI-815 can be reprogrammed by software through the JTAG/COP interface. Utilities to perform this programming are available from software development tool vendors. Additional information on the JTAG/COP interface can be found in section 3.9.

1.4 SPECIFICATIONS

Physical Characteristics — The CPCI-815 is a single slot, double high *CompactPCI*Ô peripheral card

Height:	9.187” (233.35mm) Double Eurocard (6U)
Depth:	6.299” (160mm)
Width:	.8” (20.32mm)

Power Requirements — The CPCI-815 requires +5V, +12V, -12V and +3.3V from the *CompactPCI*Ô backplane J1 connector.

The following figures represent the power consumption of the CPCI-815.

Table 1-1. CPCI-815 Power Requirements

Voltage	Current Typical
+3.3V	3.77 Amps
+5V	0.2 Amps
+12V	0.012 Amps
-12V	-0.04 Amps

1.5 ENVIRONMENTAL

The CPCI-815 should be operated in a CompactPCI card cage with good air flow. The board can be operated at ambient air temperature of 0-55 degrees Celsius, as measured at the board.

Table 1-2. ENVIRONMENTAL SPECIFICATIONS

Operating Temperatures	0 to 55 Degrees Celsius
Relative Humidity (non-condensing)	0-95%
Storage Temperatures	-55 to 125 Degrees Celsius

1.6 PHYSICAL ENVIRONMENT

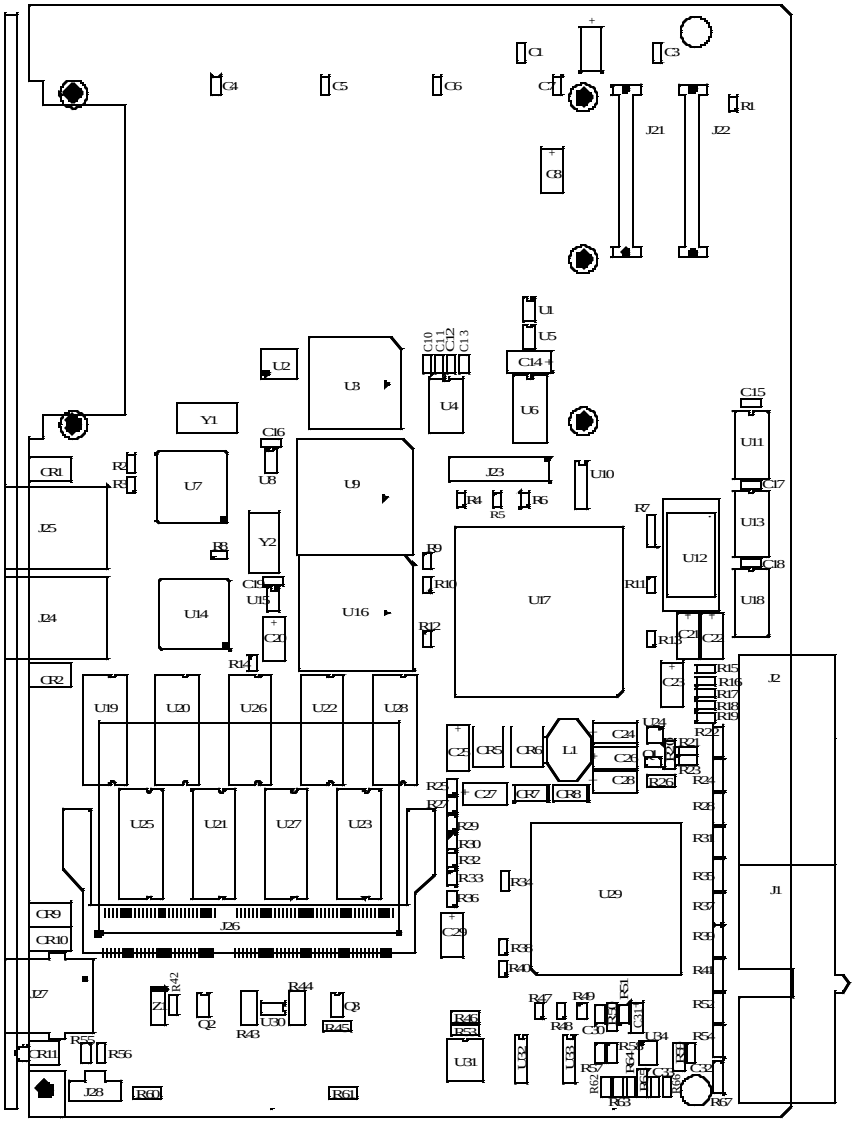

Figure 1-2. Physical Configuration

Figure 1-2 is a physical diagram of the CPCI-815 Adapter, showing the location designators of jumpers, connectors, and ICs. Refer to this figure when component locations are referenced in the manual text.

1.7 REFERENCE MANUALS

MPC8240 Integrated Processor User's Manual
Order Number MPC8240UM/D Rev. 0
Motorola Literature Distribution
P.O. Box 5405
Denver, CO 80217
(800) 441-2447

PowerPC Microprocessor Family:
The Programming Environments for 32-BIT Microprocessors, Rev. 1
Order Number MPCFPE32B/AD
Motorola Literature Distribution
P.O. Box 5405
Denver, CO 80217
(800) 441-2447

TL16C550C UART
Texas Instruments
http://www.ti.com/sc/docs/general/dsmenu.htm

LM75 Digital Temperature Sensor and Thermal Watchdog
National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
(800) 272-9959

82559ER LAN on Motherboard (LOM) Design Guide
Application Note (AP-392)
Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641
(800) 879-4683
http://www.intel.com

*CompactPCI*Ô Specification, PICMG 2.0 R3.0
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax

PCI Local Bus Specification, Revision 2.2
PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97214
(800) 433-5177 (U.S.)
(503) 693-6232 (International)
(503) 693-8344 (Fax)

I_2O Specification, Revision 1.0
I_2O Special Interest Group
(415) 750-8352
http://www.i2osig.org

*CompactPCI*Ô Hot Swap Specification, PICMG 2.1, R2.0
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax

PMC on *CompactPCI*Ô Specification, PICMG 2.0, R3.0
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax

CHAPTER 2
MPC8240 PROCESSOR

2.1 MPC8240 PROCESSOR

The MPC8240 contains a PowerPC 603e core processor. The core is configured to run at 250 MHz. This RISC processor utilizes a superscalar architecture that can issue and retire as many as three instructions per clock. The core features independent 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs).

2.2 BYTE ORDERING

The CPCI-815 is designed to run in big endian mode. The byte ordering determines how the core accesses local memory and the PCI bus. Big endian stores the most significant byte in the lowest address.

2.3 RESET VECTOR

The 8-bit wide Flash ROM is located in the address range FFE0 0000h through FFFF FFFFh. See Figure 2.1, the CPCI-815 memory map. The MPC8240 reset vector is located at address FFF0 0100h. This reset vector location, which contains a branch to the rest of the boot code, is essentially in the middle of the ROM device. This positioning results in a break up of continuous memory space and approximately 50% reduction in usable space for boot code. To better utilize this device, the CPCI-815 re-maps the reset vector to FFE0 0100h by inverting memory address 20 (A20) for the first two processor accesses to memory. These accesses are an absolute jump instruction to the beginning of boot code. After this jump A20 functions normally. Utilizing this method the majority of the 2 Mbyte Flash ROM can be used.

2.4 POWERPC MPC603E CORE CACHE, BUFFERS, ARRAYS

The processor core provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set associative, data and instruction lookaside buffers (TLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The processor also supports block address translation (BAT) arrays of four entries each.

As an added feature to the MPC603e core, the MPC8240 can lock the contents of one to three ways in the instruction and data cache (or the entire cache).

2.5 MEMORY MAP

Figure 2-1 shows the CPCI-815 memory map.

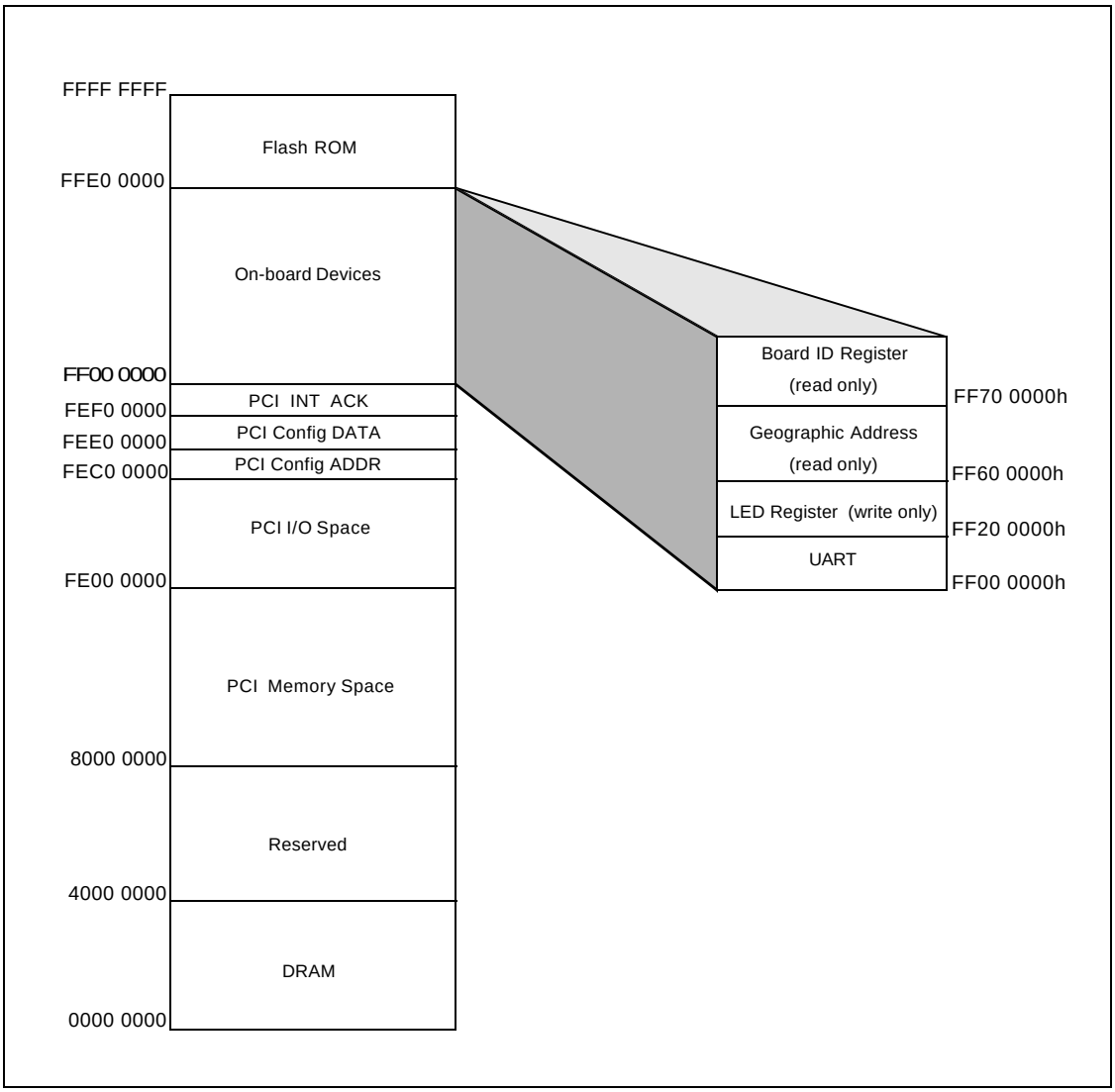

Figure 2-1. CPCI-815 Memory Map

2.6 INTERRUPTS

The CPCI-815 interrupt scheme is based upon the MPC8240 processor's embedded programmable interrupt controller (EPIC). The EPIC unit is set in the serial interrupt mode. The serial interrupt mode allows for a maximum of 16 external interrupts. Table 2-1 shows the assignment for the serial interrupts on the CPCI-815. All the interrupts are level sensitive.

The EPIC interface also contains several internal interrupt sources. These include the four global timers, the two DMA channels, the I^2C bus, and from the Message Unit.

In addition to the EPIC interface, errors detected by the MPC8240 are reported to the processor core by asserting an internal machine check signal Many of the errors detected in the MPC8240 cause exceptions to be taken by the processor core. The error reporting is provided for three of the primary interfaces, processor core interface, memory interface, and the PCI interface.

Table 2-1. Serial Interrupt Assignment

Interrupt	Interrupt Source	Polarity
0	PMC Module	0
1	PMC Module	0
2	PMC Module	0
3	PMC Module	0
4	UART	1
5	Temperature (LM75s)	0
6	Not Used	x
7	INT_BRIDGE (21554)	0
8	Ethernet 0 INT	0
9	Ethernet 1 INT	0
10	Not Used	x
11	Not Used	x
12	Not Used	x
13	Not Used	x
14	Not Used	x
15	Not Used	x

2.6.1 MPC8240 Interrupt Registers

The MPC8240 processor has several different EPIC register maps to facilitate the handling of interrupts which are briefly mentioned below. These registers occupy a 256 Kbyte range of the embedded utilities memory block (EUMB) and can be read and written by software. Please refer to the Motorola MPC8240 User's manual for more detail.

Global EPIC Registers — Provides programming control for resetting, configuration and initialization of the external interrupts. Additionally, a vector register is provided to be returned to the processor during an interrupt acknowledge cycle for a spurious vector.

Global Timer Registers — Each of the four global timers have four individual configuration registers. The registers are the Current Count register, the Base Count register, the Vector/Priority register, and the Destination register.

Interrupt Source Configuration — This group of registers are made up of the vector/priority and destination registers for the serial and internal interrupt sources. This includes the masking, polarity, and sense.

Processor-Related Registers — This group describes the processor-related EPIC registers. They are made up of the Current Task Priority register, the Interrupt Acknowledge register, and the End of Interrupt register.

2.6.2 Error Handling and Exceptions

Errors detected by the MPC8240 are reported to the processor core by asserting an internal machine check signal (mpc#). The MPC8240 detects illegal transfer types from the processor, illegal Flash write transactions, PCI address and data parity errors, accesses to memory addresses out of the range of physical memory, memory parity errors, memory refresh overflow errors, ECC errors, PCI master-abort cycles, and PCI received target-abort errors. Table 2-2 describes the relative priorities and recoverablity of externally-generated errors and exceptions.

Table 2-2. Error Priorities

Priority	Exception	Cause
0	Hard reset	Power-on reset, CompactPCI chassis reset switch or via JTAG controller
1	Machine check	Processor transaction error or Flash error
2	Machine check	PCI address parity error or PCI data parity error when the CPCI-815 is acting as the PCI target
3	Machine check	Memory select error, memory refresh overflow, or ECC error
4	Machine check	PCI address parity error or PCI data parity error when the CPCI-815 is acting as the PCI master, PCI master-abort, or received PCI target-abort

CHAPTER 3
HARDWARE

3.1 SDRAM

The CPCI-815 is equipped with 64 Mbytes of ECC SDRAM. The memory is made up of nine 64 Mbit (8M x 8) devices in an 8M by 72-bit configuration.

The memory controller unit (MCU) of the CPCI-815 supports SDRAM burst lengths of four. A burst length of four enables seamless read/write bursting of long data streams as long as the MCU does not cross the page boundary. Page boundaries are naturally aligned 2 Kbyte blocks. 72-bit SDRAM with ECC running at 100 MHz allows a maximum throughput of 800 Mbytes per second. The MCU keeps four pages open simultaneously. Simultaneously open pages allow for greater performance for sequential access, distributed across multiple internal bus transaction.

3.1.1 Upgrading SDRAM

The CPCI-815 is equipped with 64 Mbytes of SDRAM with ECC mounted on the card. The memory may be expanded by inserting an additional 16 Mbyte to 128 MByte module into the 144 pin SoDIMM socket. Only 144 pin +3.3V SDRAM modules with or without ECC rated for 100 MHz operation should be used on the CPCI-815.

3.1.2 SDRAM Configurations Installation and Removal of Memory Modules

Installation or removal of DIMMs on the CPCI-815 is a simple procedure and requires no special tools. The CPCI-815 should be removed from the host system before its memory configuration is changed, and care must be taken to avoid static discharge while contacting the board. A properly connected grounding strap should be worn while installing or removing memory modules on the CPCI-815 adapter.

Memory modules are removed by rotating the latches located on each end of the SoDIMM socket outward, away from the module. As the latches are moved outward, the module will be ejected from the socket.

To install a memory module, first identify its proper orientation. Each module is keyed with a pair of notches in the card edge of the PC board that correspond to tabs in the socket. With the correct orientation established and the latches in their outward position, begin to slide the module into the socket. The two card edge corners of the module mate with the slots in each latch first. By pressing the module and socket together, the module should snap into the socket. Check that the latches are in their fully closed (inward) position.

3.2 FLASH ROM

The CPCI-815 provides 2 Mbytes of sector-programmable Flash ROM for non-volatile code storage. The Flash ROM is located in local memory space at address FFE0 0000h through FFFF FFFFh. The mapping ensures that, after a reset, the MPC8240 processor can execute the hard reset exception handler located at FFF0 0100h.

3.2.1 Non-Volatile Parameter Memory

One 64 Kbyte sector of the Flash ROM on the CPCI-815 is reserved for the storage of application parameters. The boot parameter block is divided into 4 Kbyte sections, each of which may be used for the storage of a set of boot parameters.

3.3 CONSOLE SERIAL PORT

A single console serial port with an RS-232 line interface has been included on the CPCI-815. The port is connected to a RJ-11 style phone jack on the adapter, and can be connected to a host system using the included phone jack to DB-25 cable (Cyclone P/N 530-2006). The pinout of the console connector is as shown in Table 3-1.

Table 3-1. Console Port Connector

Pin	Signal	Description
1		Not Used
2	GND	Ground
3	TXD	Transmit Data
4	RXD	Receive Data
5		Not Used
6		Not Used

Note

Pin 1 is the contact to the extreme left looking into the console port opening with the tab notch facing down.

The serial port is based on a 16C550 UART clocked at 1.843 MHz. The device may be programmed to use this clock with the internal baud rate counters. The serial port is capable of operating at speeds from 300 to 115200 bps, and can be operated in interrupt-driven or polled mode. The 16C550 register set is shown in Table 3-2. For a detailed description of the registers and device operation refer to the 16C550 databook.

Table 3-2. UART Register Addresses

Address	Read Register	Write Register
FF00 0000H	Receive Holding Register	Transmit Holding Register
FF00 0008H	Unused	Interrupt Enable Register
FF00 0010H	Interrupt Status Register	FIFO Control Register
FF00 0018H	Unused	Line Control Register
FF00 0020H	Unused	Modem Control Register
FF00 0028H	Line Status Register	Unused
FF00 0030H	Modem Status Register	Unused
FF00 0038H	Scratchpad Register	Scratchpad Register

3.4 COUNTER/TIMERS

The MPC8240 processor is equipped with four 31-bit on-chip counter/timers which count at 1/8 the frequency of the SDRAM_CLK signal or 12.5MHz. Users should refer to the Processor User's Manual for the functionality and programming of the counters. The timers can be individually programmed to generate interrupts to the processor when they count down to zero. Two of the timers, timer2 and timer3, can be set up to automatically start periodic DMA operations for DMA channels 0 and 1, respectively, without using the processor interrupt mechanism.

3.5 LEDS

The CPCI-815 has eight green LEDs and one blue LED. The four green LEDs labeled, IOP, ACT, STAT0, and STAT1 are under software control. The LEDs are controlled by a write-only register, which is located at address FF20 0000H. The LED Register bitmap is shown in Figure 3-1.

Two green LEDs labeled 'LNK' are associated with the Ethernet ports '0' and '1' and indicate link integrity. The remaining two LEDs labeled 'ACT' indicate network activity for the corresponding ports.

The blue LED indicates Hot Swap operations. Refer to section 3.13.1 for additional information.

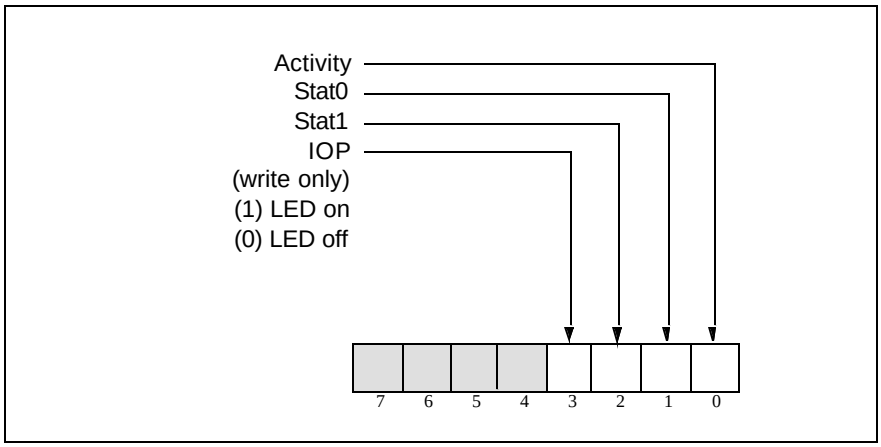

Figure 3-1. LED Register Bitmap, FF20 0000H

3.6 PCI INTERFACE

The CPCI-815 contains a primary 64-bit PCI bus and a secondary 32-bit PCI bus. Both buses are clocked at 33 MHz. The primary PCI bus interfaces the 64-bit CompactPCI bus to the 21154 PCI-to-PCI bridge. The other side of the 21554 interfaces a 32-bit PCI bus to the MPC8240.

3.6.1 Primary PCI Arbitration

The primary PCI bus arbitration is provided by the host of the CompactPCI system.

3.6.2 Secondary PCI Arbitration

Secondary bus arbitration logic between the MPC8240 processor, the 21554 bridge, the two ethernet interfaces and the two PMC devices, is contained within the MPC8240. The bus arbitration unit allows fairness as well as a priority mechanism. A two-level round-robin scheme is used in which each device can be programmed within a pool of high- or low-priority arbitration. One member of the low-priority pool is promoted to the high-priority pool. As soon as it is granted the bus it returns to the low-priority pool.

3.7 DMA CHANNELS

The MPC8240 processor features two DMA channels. Data movement occurs on the PCI and/or memory bus. Each channel has a 64-byte queue to facilitate the gathering and sending of data. Both the local processor and PCI masters can initiate a DMA transfer. Some of the features of the MPC8240 DMA unit include: misaligned transfer capability, scatter gather DMA chaining and direct DMA modes, and interrupt on completed segment, chain, and error. Figure 3-2 provides a block diagram of the MPC8240 DMA unit.

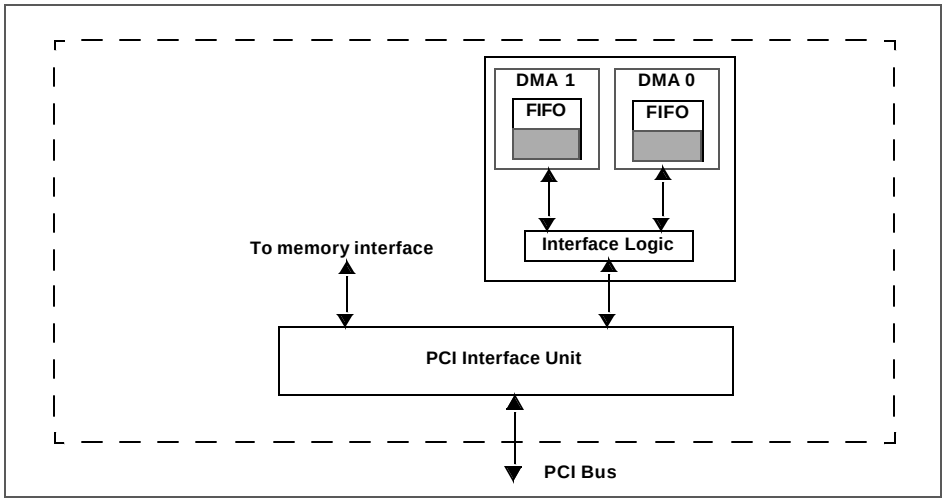

Figure 3-2. MPC8240 Processor DMA Controller

3.8 MESSAGE UNIT

The MPC8240 provides a message unit (MU) to facilitate communications between the host processor and peripheral processors. The MPC8240's MU can operate with generic messages and doorbell registers, and also implements an I_2O compliant interface.

The Intelligent Input Output (I_2O) specification allows architecture-independent I/O subsystems to communicate with an OS through an abstraction layer. The specification is centered around a message-passing scheme. An I_2O-compliant peripheral (IOP) is comprised of memory, processor, and input/output devices. The IOP dedicates a certain space in its local memory to hold inbound (from the remote processor) and outbound (to the remote processor) messages. The space is managed as memory-mapped FIFOs with pointers to this memory maintained through the MPC8240 I_2O registers. Please refer to the MPC8240 User's Manual for I_2O register descriptions, FIFO descriptions and an I_2O message queue example.

3.9 JTAG/COP SUPPORT

The MPC8240 provides a joint test action group (JTAG) interface. Additionally, the JTAG interface is also used for accessing the common on-chip processor (COP) function of PowerPC processors. The COP function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor. The 16 pin COP header (sample part is Samtec # HTSW-108-07-S-S) is located at J23. The COP header adds many benefits including breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface. The COP header definition is shown in Figure 3-3 and Table 3-3. The location of pin 1 on the header is indicated by the "dot" on the top right corner of J23, which is shown in Figure 1-2.

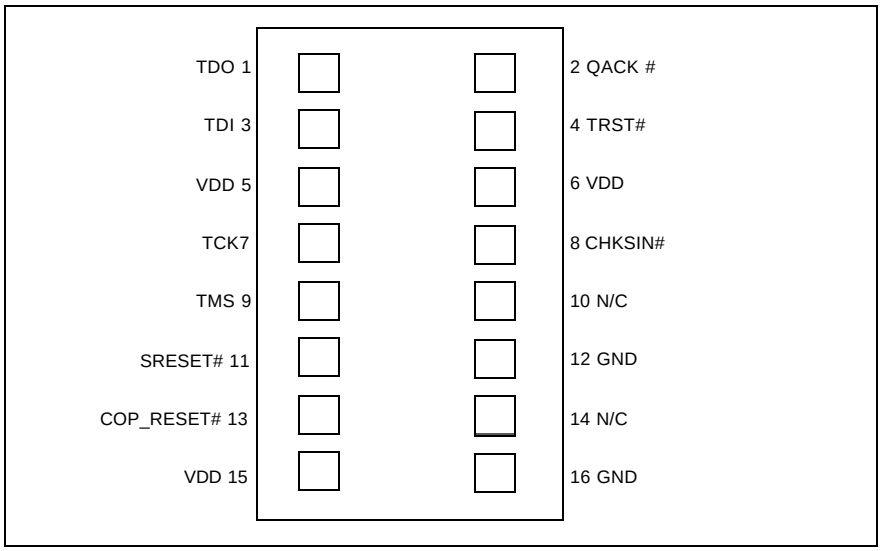

Figure 3-3. COP Header

Table 3-3. JTAG/COP Pin Assignment

Signal	Pin	Pin	Signal
TDO	1	2	QACK#
TDI	3	4	TRST#
Pull-up to +3V	5	6	+3V
TCK	7	8	CHKSTOPIN#
TMS	9	10	N/C
SRESET#	11	12	GND
COP_RESET#	13	14	N/C
Pull-up to +3V	15	16	GND

3.10 I²C BUS

The CPCI-815 has two components attached to the Inter-Integrated Circuit (I^2C) bus interface of the MPC8240 processor: the SoDIMM SDRAM EEPROM and two temperature sensors. The I^2C addresses of the devices are shown in Table 3-4.

Table 3-4. I²C Device Addresses

Designator	Device	Function	Address
U1	LM75	Temperature Sensor	1001000
U5	LM75	Temperature Sensor	1001000
J26	SoDIMM EEPROM	Temperature Sensor	1001001

3.10.1 Temperature Sensors

The LM75 temperature sensors have overtemperature trip points that will trigger an interrupt when crossed. The sensors have been placed on the board at U1 and U5, and share serial interrupt #5. The sensors are placed in the interrupt mode by the Breeze initialization code. The Breeze default overtemperature point is 55 degrees Celsius. The sensors can be read for a temperature reading at any time, and reading after and interrupt clears the interrupt. The sensor will not interrupt again until the temperature has dropped below the hysteresis (default is 50 degrees Celsius). Consult the LM75 data sheet for more details on programming the temperature sensors.

3.11 ETHERNET PORTS

The two Ethernet ports are based on the Intel 82559ER Fast Ethernet PCI Bus LAN Controller with Integrated PHY (physical layer interface) and support 10BaseT or 100BaseTx signaling. If 100BaseTx signaling is negotiated with its link partner, the port will perform serial transfer at 100 Mbps. The 82559ER is the core component of the Ethernet interface. It uses a 32-bit PCI interface to communicate with the host and has an integrated PHY that connects via an isolation transformer to the network.

3.11.1 82559ER Ethernet Controller

The 82559ER is an integrated 32-bit PCI LAN controller for 10/100Mbps Fast Ethernet networks. It consists of both the Media Access Controller (MAC) and the 10/100 Mbps physical layer interface (PHY).

The integrated PHY supports 10BaseT and 100BaseTx operation. The PHY performs digitally controlled receive line equalization and transmit waveform generation for 10Mbps and 100Mbps Ethernet networks.

The MAC is a 32-bit PCI bus master with enhanced scatter-gather memory operations without CPU intervention. Three kilobyte transmit and receive FIFOS provide storage of multiple transmit and receive frames.

3.11.2 Ethernet Port LEDs

The Ethernet ports on the CPCI-815 each have two LEDs driven by associated 82559 that provide a visual indication of network status:

The LEDs labeled ‘LNK’ indicate link integrity for Ethernet port 0 and port 1. The ‘LNK’ LEDs will be ON continuously if the port is connected to a functional network or Ethernet port.

The LEDs labeled ‘ACT’ indicate network activity for the corresponding port. The ‘ACT’ LEDs will blink during transmit or receive activity.

3.11.3 Ethernet Port Connector

Each Ethernet port is connected to a shielded RJ45 (modular phone type) connector. The connector conforms to the 10/100BaseTx specification. The connector exits the front panel of the CPCI-815. The ports (and LEDs) are labeled on the front panel. The pinout of each is shown in Table 3-5. Pin 1 is to the extreme left as you look into the connector opening with the tab notch down.

Table 3-5. 100BaseTx Connector

Pin	Signal	Description
1	TX+	Output
2	TX-	Output
3	RX+	Input
4		Not Used
5		Not Used
6	RX-	Input
7		Not Used
8		Not Used

3.12 HOT SWAP

The CPCI-815 is a PICMG 2.1 compliant Hot Swap board. THe CPCI-815 is a “Full Hot Swap” board with both hardware and software connection control. The CPCI-815 can be used on all platform types; non-Hot Swap platform for a conventional system, Hot Swap platform for a Full Hot Swap system, and High Availability platform for a High Availability system. See the Hot Swap specification for further explanation of platform, board and system types.

3.12.1 Hot Swap Extraction Process

Removal of the CPCI-815 in a Full Hot Swap or High Availability system is the same. The operator first only opens the ejector handles of the board. A switch on the CPCI-815 signals to the system that it is to be extracted. In response, the system will illuminate the blue Hot Swap LED when extraction is permitted.

3.12.2 Hot Swap Insertion Process

Insertion of the CPCI-815 is the same in any Hot Swap system. The operator merely slides the CPCI-815 into the desired slot and latches the handles.

3.13 BOARD ID REGISTER

The Board ID Register is a read-only register that can be used to differentiate between the CPCI-815 and other Cyclone Microsystems MPC8240-based CompactPCI cards. It is located at address FF70 0000h on all such cards, with each card returning a unique ID value. Figure 3-4 shows the board ID for the CPCI-815.

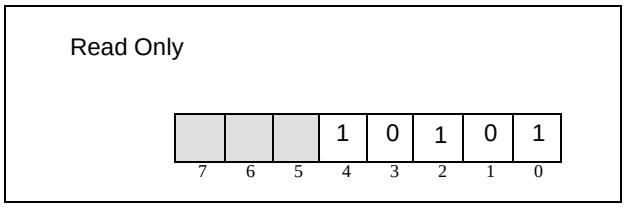

Figure 3-4. Board Identification Registers, FF70 0000h

APPENDIX A
PMC MODULE INTERFACE

A.1 INTRODUCTION

The PMC Module Interface allows PCI devices to be connected to the secondary PCI interface of the CPCI-815 Adapter. The IEEE STD P1386.1, PCI Mezzanine Card (PMC), provides for one set of clocking and arbitration signals per PMC Module. Cyclone Microsystems has expanded this to two sets for the PMC Module on the CPCI-815. Otherwise, with a few exceptions, the standard signals defined for 32-bit CPCI connectors are used for the PMC Modules. The exceptions are noted in section A.3. The timing for devices on PMC Modules is the same as the timing for any other PCI device; see the *PCI Local Bus Specification* revision 2.1 for details.

A number of PMC Modules are available from Cyclone Microsystems. This section is intended for users interested in developing their own modules.

A.2 PHYSICAL ATTRIBUTES

Please refer to IEEE P1386/Draft 2.0 for the physical dimensions of PMC modules.

A.3 PMC MODULE SIGNAL DEFINITIONS

PMC Modules use the signals defined in the IEEE STD P1386.1. The following four signals are added to this definition to handle the expansion from one to three devices per PMC module:

- GNT1#
- REQ1#
- CLK1
- IDSEL1

Please note that the added signals used the PMC-RSVD signals as defined in IEEE STD P1386.1. The PCI-RSVD remain untouched.

Also, note that GNT1# follow the description for GNT#, REQ1# follow the description for REQ#, CLK1 follow the description for CLK, and IDSEL1 follow the description for IDSEL. When the appropriate signals are connected to PCI devices on a PMC Module, each device has the full complement of PCI signals defined in the specification.

Table A-1 shows the IDSELx# routing and Table A-2 shows the interrupt routing on the CPCI-815.

Table A-1. PMC Clock & Arbitration Assignment

IDSEL	ADDR	IDSEL#	CLOCK	ARBITRATION
IDSEL#	AD16	J12.25	CLKA	REQ0#,GNT0#
IDSEL1#	AD17	J12.34	CLKB	REQ1#,GNT1#

Table A-2. PMC Interrupt Assignment

DEVICE INTx#	1ST DEVICE	2ND DEVICE
INTA#	INTA#	INTD#
INTB#	INTB#	INTA#
INTC#	INTC#	INTB#
INTD#	INTD#	INTC#

A.4 PMC MODULE CONNECTOR

PMC Modules use three board-to-board connectors (plug) with 64 pins each. The receptacles (AMP P/N 120521-2) is located on the host platform and attaches to the plugs (AMP P/N 120527-2). This connector combination allows for a 10 mm board-to-board spacing. See IEEE P1386/Draft 2.0 for dimensions and component clearance details.

Table A-3. P21 PMC Module Connector Pinout

Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	PCI-RSVD
11	GND	12	PCI-RSVD
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V(I/O)	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5V
31	V(I/O)	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	SDONE#	42	SBO#
43	PAR	44	GND
45	V(I/O)	46	AD15

47	AD12	48	AD11
49	AD09	50	+5V
51	GND	52	C/BE0#
53	AD06	54	AD05
55	AD04	56	GND
57	V(I/O)	58	AD03
59	AD02	60	AD01
61	AD00	62	+5V
63	GND	64	REQ64#

Table A-4. P22 PMC Module Connector Pinout

Pin	Signal	Pin	Signal
1	+12V	2	TRST#
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	PCI-RSVD
9	PCI-RSVD	10	PCI-RSVD
11	BUSMODE2#	12	+3.3V
13	RST#	14	BUSMODE3#
15	+3.3V	16	BUSMODE4#
17	PCI-RSVD	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3V
25	IDSEL	26	AD23
27	+3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	PMC+IDSEL1
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD08	50	+3.3V
51	AD07	52	PMC+REQ1

53	+3.3V	54	PMC+CLK1
55	PMC+GNT1#	56	GND
57	PMC-RSVD	58	PMC-RSVD
59	GND	60	PMC-RSVD
61	ACK64#	62	+3.3V
63	GND	64	PMC-RSVD