COMPACT PCI-811
SERIAL I/O
CONTROLLER
USER'S MANUAL

Revision 1.0, October 2001

Cyclone P/N 800-0811

CHAPTER 1

CHAPTER 2

CHAPTER 3

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1
GENERAL INTRODUCTION

1.1 INTRODUCTION

The CPCI-811 is a high-performance CompactPCI peripheral board featuring up to eight high-speed serial ports. A block diagram is shown in Figure 1-1.

The board is based on the MPC8240 PowerPC™ integrated processor. The MPC8240 has a processor core based on the PowerPC603e™ low-power microprocessor, and also performs many peripheral functions on chip. The peripheral logic integrates a PCI bridge, memory controller, DMA controller, interrupt controller, I_2O controller, and an I^2C controller.

Additionally, the CPCI-811 high speed serial ports are software configurable for V.35 or EIA-530A signaling.

Software development tools for PowerPC processors are available from a variety of vendors, and Board Support Packages (BSPs) for the pSOS operating system are available from Cyclone.

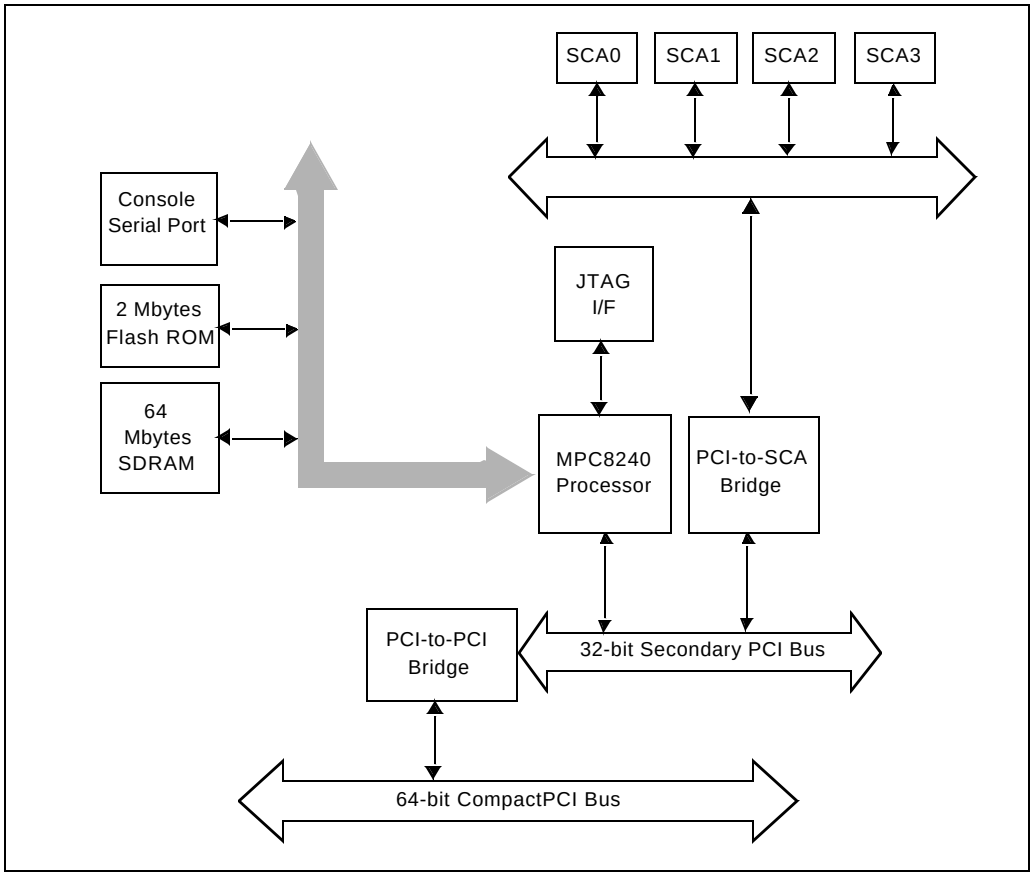

Figure 1-1. CPCI-811 Block Diagram

1.2 FEATURES

- MPC8240 Processor — The microprocessor is Motorola's integrated MPC8240 PowerPC. The device integrates a Motorola 32-bit superscalar PowerPC 603e core, running at 250 MHz internally, and Peripheral Components Interconnect (PCI). The core boasts a 16 Kbyte instruction cache, a 16 Kbyte data cache and floating-point support. Memory can be accessed through the memory controller to the core processor or from the PCI bus.
- 21554 PCI-to-PCI Bridge — The 21554 is a "non-transparent" PCI-to-PCI bridge with a 64-bit primary bus interface and a 64-bit secondary interface. A non-transparent bridge allows the local processor to configure and control the local subsystem. The 21554 primary bus interfaces with the 64-bit CompactPCI bus and the secondary bus interfaces with the 32-bit PCI bus of the MPC8240.
- SDRAM — 64 MBytes of SDRAM is standard on the CPCI-811.
- Four Port Module — A factory installed module expands the number of high speed serial ports on the CPCI-811 from four to eight. An eight port CPCI-811 occupies two CompactPCI slots.
- *CompactPCI* Interface — The CPCI-811 meets the PICMG Rev. 2.0 Specification for system slot adapters. The PCI bus runs at 33MHz.
- Flash ROM — 2 Mbytes of in-circuit sector-programmable Flash ROM.
- Console Serial Port — An RS-232 serial port is provided for a console terminal or workstation connection. The serial port supports up to 115 Kbps and uses a phone jack to DB25 cable supplied with the CPCI-811 board.
- High Speed Serial Ports — Four or eight high speed serial ports, based on the Hitachi HD64570 Serial Communications Adapter (SCA). The line interface of the ports is software selectable between V.35 or EIA-530A. Connectors are EIA-530-A, Alt-A (26 position) type.
- Hot Swap — The CPCI-811 is a Full Hot Swap board, compliant with PICMG 2.1.
- Timers — Four 31-bit timers are available to generate interrupts.
- DMA Controller — The MPC8240 supports 2 separate DMA channels for high throughput data transfers between PCI bus agents and the local SDRAM memory.
- I_2O Messaging — The CPCI-811 supports the I_2O specification for interprocessor communication.

1.3 OVERVIEW

The CPCI-811 is a 6U CompactPCI peripheral board with support for four or eight high speed serial ports. The four port CPCI-811 occupies one slot in a CompactPCI chassis. A daughter card, with four additional ports is added to create the eight port version, which occupies two chassis slots.

The CPCI-811 has two PCI buses, a primary and a secondary. The primary PCI bus is the CompactPCI bus. The secondary PCI bus is a local bus that supports the MPC8240 and a PLX PCI9080 bridge to the Hitachi SCAs. (The SCA devices do not have a PCI interface, so another bridge is used to interface them to the MPC8240).

The CPCI-811 uses an Intel 21554 Embedded PCI-to-PCI Bridge to bridge between the primary CompactPCI bus and the secondary local PCI bus. This device complies with the PCI Local Bus Specification, revision 2.1. It provides concurrent bus operation, allows buffering for both read and write transactions and provides support for Hot Swap operation.

The primary PCI interface is 64-bit data but will operate correctly when the CPCI-811 is plugged into a 32-bit CompactPCI slot. Although the secondary PCI bus of the 21554 is 64-bit data, the local bus of the CPCI-811 is 32-bit, and the MPC8240 and PCI9080 are 32-bit PCI devices. The data path to memory of the CPCI-811 is 64-bit. The memory controller resides on the MPC8240.

The Flash ROM on the CPCI-811 can be reprogrammed by software through a JTAG/COP interface. Utilities to perform this programming are available from software development tool vendors. Additional information on the JTAG/COP interface can be found in section 3.9.

1.4 SPECIFICATIONS

Physical Characteristics

The four port CPCI-811 is a single slot, double high *CompactPCI*Ô peripheral card. The eight port CPCI-811 is a two slot, double high *CompactPCI*Ô peripheral card.

Height:	9.187” (233.35mm) Double Eurocard (6U)
Depth:	6.299” (160mm)
Width:	0.8” (20.32mm) Four Port version.
Width:	1.6” (40.64mm) Eight Port version.

Power Requirements

The CPCI-811 requires +5V, +12V and +3.3V from the *CompactPCI*Ô backplane J1 connector.

The following figures represent the power consumption of the eight port version of the CPCI-811.

Table 1-1. CPCI-811 Power Requirements

Voltage	Current Typical	Current Maximum
+3.3V	1.875 Amps	2.708 Amps
+5V	2.773 Amps	3.772 Amps
+12V	0.02 Amps	0.03 Amps
-12V	0 Amps	0 Amps

1.5 ENVIRONMENTAL

The CPCI-811 should be operated in a CompactPCI card cage with good air flow. The board can be operated at ambient air temperature of 0-55 degrees Celsius, as measured at the board.

Table 1-2. ENVIRONMENTAL SPECIFICATIONS

Operating Temperatures	0 to 55 Degrees Celsius
Relative Humidity (non-condensing)	0-95%
Storage Temperatures	-55 to 125 Degrees Celsius

1.6 PHYSICAL ENVIRONMENT

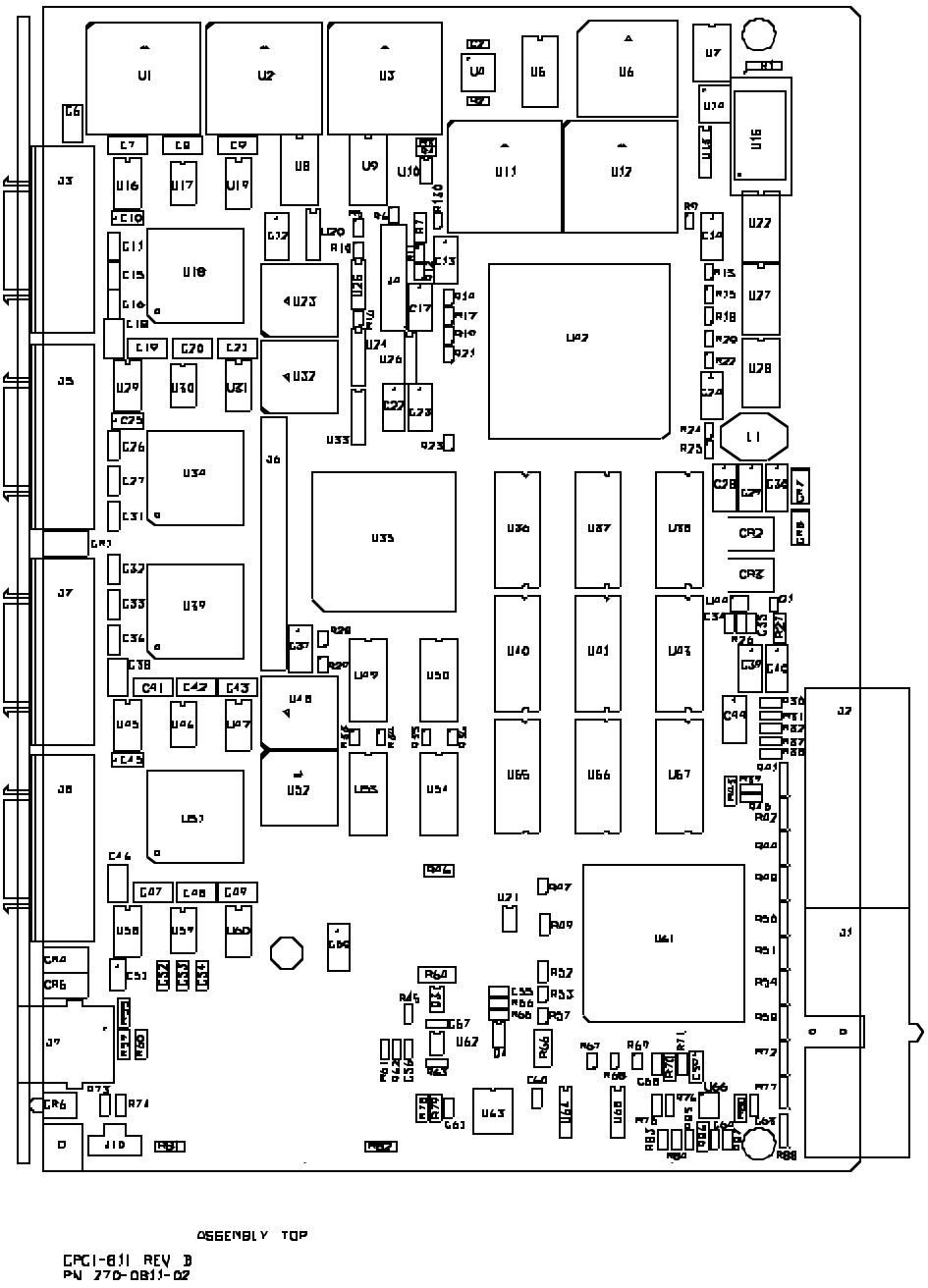

Figure 1-2. Physical Configuration

Figure 1-2 is a physical diagram of the CPCI-811, showing the location designators of jumpers, connectors, and ICs. Refer to this figure when component locations are referenced in the manual text.

1.7 REFERENCE MANUALS

MPC8240 Integrated Processor User's Manual
Order Number MPC8240UM/D Rev. 0
Motorola Literature Distribution
P.O. Box 5405
Denver, CO 80217
(800) 441-2447

PowerPC Microprocessor Family:
The Programming Environments for 32-bit Microprocessors, Rev. 1
Order Number MPCFPE32B/AD
Motorola Literature Distribution
P.O. Box 5405
Denver, CO 80217
(800) 441-2447

TL16C550C UART
Texas Instruments
http://www.ti.com/sc/docs/general/dsmenu.htm

PCI-9080
PLX Technology, Inc.
390 Potrero Avenue
Sunnyvale, CA 94086
(800) 759-3735
(408) 774-2169 Fax
http://www.plxtech.com

HD64570 Serial Communications Adapter (SCA) User's Manual
Hitachi American, LTD
Semiconductor Division
Hitachi Plaza
2000 Sierra Point Parkway
Brisbane, CA 94005-1819

LM75 Digital Temperature Sensor and Thermal Watchdog
National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
(800) 272-9959

CompactPCI® Specification
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax

PCI Local BIOS Specification, Revision 2.1
PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97214
(800) 433-5177 (U.S.)
(503) 693-6232 (International)
(503) 693-8344 (Fax)

I_2O Specification, Revision 1.0
I_2O Special Interest Group
(415) 750-8352
http://www.i2osig.org

CompactPCI® Hot Swap Specification, PICMG 2.1, R1.0
PCI Industrial Computers Manufacturing Group
301 Edgewater Place, Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 Fax

CHAPTER 2
MPC8240 PROCESSOR

2.1 MPC8240 PROCESSOR

The MPC8240 contains a PowerPC 603e core processor. The core is configured to run at 250 MHz. This RISC processor utilizes a superscalar architecture that can issue and retire as many as three instructions per clock. The core features independent 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs).

2.2 BYTE ORDERING

The CPCI-811 is designed to run in big endian mode. The byte ordering determines how the core accesses local memory and the PCI bus. Big endian stores the most significant byte in the lowest address.

2.3 RESET VECTOR

The 8-bit wide Flash ROM is located in the address range FFE0 0000h through FFFF FFFFh. See Figure 2-1, the CPCI-811 memory map. The MPC8240 reset vector is located at address FFF0 0100h. This reset vector location, which contains a branch to the rest of the boot code, is essentially in the middle of the ROM device. This positioning results in a break up of continuous memory space and approximately 50% reduction in usable space for boot code. To better utilize this device, the CPCI-811 re-maps the reset vector to FFE0 0100h by inverting memory address 20 (A20) for the first two processor accesses to memory. These accesses are an absolute jump instruction to the beginning of boot code. After this jump, A20 functions normally. Utilizing this method, the majority of the 2 Mbyte Flash ROM can be used.

2.4 POWERPC MPC603E CORE CACHE, BUFFERS, ARRAYS

The processor core provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data, and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set associative, data and instruction lookaside buffers (TLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The processor also supports block address translation (BAT) arrays of four entries each.

As an added feature to the MPC603e core, the MPC8240 can lock the contents of one to three ways in the instruction and data cache (or the entire cache).

2.5 MEMORY MAP

Figure 2-1 shows the CPCI-811 memory map.

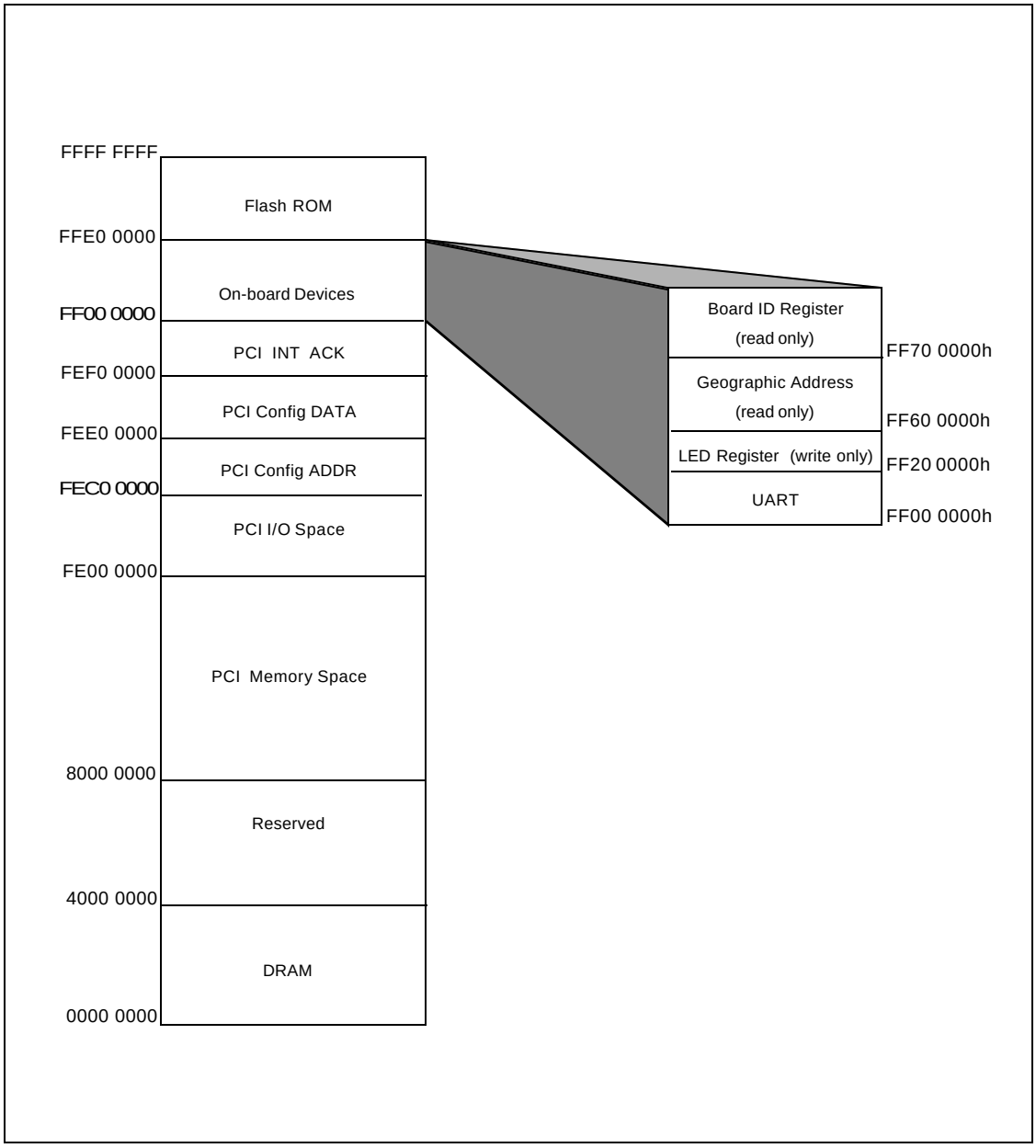

Figure 2-1. CPCI-811 Memory Map

2.6 INTERRUPTS

The CPCI-811 interrupt scheme is based upon the MPC8240 processor's embedded programmable interrupt controller (EPIC). The EPIC unit is set to serial interrupt mode. Serial interrupt mode allows for a maximum of 16 external interrupts. Table 2-1 shows the assignment of devices to serial interrupts on the CPCI-811, all the interrupts are level sensitive.

The EPIC interface also contains several internal interrupt sources. These include the four global timers, the two DMA channels, the I^2C bus, and from the Message Unit.

In addition to the EPIC interface, errors detected by the MPC8240 are reported to the processor core by asserting an internal machine check signal Many of the errors detected in the MPC8240 cause exceptions to be taken by the processor core. The error reporting is provided for three of the primary interfaces, processor core interface, memory interface, and the PCI interface.

Table 2-1. Serial Interrupt Assignment

INTERRUPT	INTERRUPT SOURCE	POLARITY
0	SCA 0	0
1	SCA 1	0
2	SCA 2	0
3	SCA 3	0
4	UART	1
5	Temperature (LM75s)	0
6	LSERR (PCI9080)	0
7	SINT A (21554)	0
8	Not Used	X
9	Not Used	X
10	Not Used	X
11	Not Used	X
12	Not Used	X
13	Not Used	X
14	Not Used	X
15	Not Used	X

2.6.1 MPC8240 Interrupt Registers

The MPC8240 processor has several different EPIC register maps to facilitate the handling of interrupts which are briefly mentioned below. These registers occupy a 256Kbyte range of the embedded utilities memory block (EUMB) and can be read and written by software. Please refer to the Motorola MPC8240 User's Manual for more detail.

Global EPIC Registers — Provides programming control for resetting, configuration and initialization of the external interrupts. Additionally, a vector register is provided to be returned to the processor during an interrupt acknowledge cycle for a spurious vector.

Global Timer Registers — Each of the four global timers have four individual configuration registers. The registers are the Current Count register, the Base Count register, the Vector/Priority register, and the Destination register.

Interrupt Source Configuration	This group of registers are made up of the vector/priority and destination registers for the serial and internal interrupt sources. This includes the masking, polarity, and sense.
Processor-Related Registers	This group describes the processor-related EPIC registers. They are made up of the Current Task Priority register, the Interrupt Acknowledge register, and the End of Interrupt register.

2.6.2 Error Handling and Exceptions

Errors detected by the MPC8240 are reported to the processor core by asserting an internal machine check signal (mcp#). The MPC8240 detects illegal transfer types from the processor, illegal Flash write transactions, PCI address and data parity errors, accesses to memory addresses out of the range of physical memory, memory parity errors, memory refresh overflow errors, ECC errors, PCI master-abort cycles, and PCI received target-abort errors. Table 2-2 describes the relative priorities and recoverablity of externally-generated errors and exceptions.

Table 2-2. Error Priorities

Priority	Exception	Cause
0	Hard reset	Power-on reset, CompactPCI chassis reset switch or via JTAG controller
1	Machine check	Processor transaction error or Flash error
2	Machine check	PCI address parity error or PCI data parity error when the CPCI-811 is acting as the PCI target
3	Machine check	Memory select error, memory refresh overflow, or ECC error
4	Machine check	PCI address parity error or PCI data parity error when the CPCI-811 is acting as the PCI master, PCI master-abort, or received PCI target-abort

2.7 SCA SIDE DEVICE MAP

A PLX PCI9080 is used to bridge the Hitachi SCAs to the Secondary PCI bus. (The SCAs devices do not have a PCI interface, so another bridge is used to interface them to the MPC8240). The SCAs and associated registers can be accessed through the PCI9080's local address space 0. User software can access the SCAs by reading the value of the PCIBAR2 register in the PCI 9080's PCI configuration space, then adding the appropriateoffset as listed in Table 2-3.

Table 2-3. SCA SIDE DEVICE MAP

Offset from PCI9080 BAR2	Device or Function
7000h	Select Transmit clocks inbound
6000h	Select Transmit clocks outbound
5000h	Select EIA530A line interface
4000h	Select V.35 line interface
0F00h	Deassert SCA3 reset
0E00h	Assert SCA3 reset
0D01h	SCA3 Interrupt Acknowledge
0CFFh through 0C00h	SCA3 Registers
0B00h	Deassert SCA2 reset
0A00h	Assert SCA2 reset
0901h	SCA2 Interrupt Acknowledge
08FFh through 0800h	SCA2 Registers
0700h	Deassert SCA1 reset
0600h	Assert SCA1 reset
0501h	SCA1 Interrupt Acknowledge
04FFh through 0400h	SCA1 Registers
0300h	Deassert SCA0 reset
0200h	Assert SCA0 reset
0101h	SCA0 Interrupt Acknowledge
00FFh through 0000h	SCA0 Registers

CHAPTER 3
HARDWARE

3.1 SDRAM

The CPCI-811 is equipped with 64M bytes of SDRAM mounted on the card. The memory is made up of four, 128Mbit (8M x 16) devices in an 8M by 64-bit configuration.

The memory controller unit (MCU) of the CPCI-811 supports SDRAM burst lengths of four. A burst length of four enables seamless read/write bursting of long data streams as long as the MCU does not cross the page boundary. Page boundaries are naturally aligned 2 Kbyte blocks. 64-bit SDRAM running at 100MHz allows a maximum throughput of 800 Mbytes per second. The MCU keeps four pages open simultaneously. Simultaneously open pages allow for greater performance for sequential access, distributed across multiple internal bus transaction.

3.2 FLASH ROM

The CPCI-811 provides 2 Mbytes of sector-programmable Flash ROM for non-volatile code storage. The Flash ROM is located in local memory space at address FFE0 0000h through FFFF FFFFh. The mapping ensures that, after a reset, the MPC8240 processor can execute the hard reset exception handler located at FFF0 0100h.

3.3 CONSOLE SERIAL PORT

A single console serial port with an RS-232 line interface has been included on the CPCI-811. The port is connected to a RJ-11 style phone jack on the adapter, and can be connected to a host system using the included phone jack to DB-25 cable (Cyclone P/N 530-2002). The pinout of the console connector is as shown in Table 3-1.

Table 3-1. Console Port Connector

Pin	Signal	Description
1		Not Used
2	GND	Ground
3	TXD	Transmit Data
4	RXD	Receive Data
5		Not Used
6		Not Used

K Note

Pin 1 is the contact to the extreme left looking into the console port opening, with the tab notch facing down.

The serial port is based on a 16C550 UART clocked at 1.843 MHz. The device may be programmed to use this clock with the internal baud rate counters. The serial port is capable of operating at speeds from 300 to 115200 bps, and can be operated in interrupt-driven or polled mode. The 16C550 register set is shown in Table 3-2. For a detailed description of the registers and device operation refer to the 16C550 databook.

Table 3-2. Register Addresses

Address	Read Register	Write Register
FF00 0000H	Receive Holding Register	Transmit Holding Register
FF00 0008H	Unused	Interrupt Enable Register
FF00 0010H	Interrupt Status Register	FIFO Control Register
FF00 0018H	Unused	Line Control Register
FF00 0020H	Unused	Modem Control Register
FF00 0028H	Line Status Register	Unused
FF00 0030H	Modem Status Register	Unused
FF00 0038H	Scratchpad Register	Scratchpad Register

3.4 COUNTER/TIMERS

The MPC8240 processor is equipped with four 31-bit on-chip counter/timers which count at 1/8 the frequency of the SDRAM clock signal or 12.5MHz. Users should refer to the MPC8240 User's Manual for the functionality and programming of the counters. The timers can be individually programmed to generate interrupts to the processor when they count down to zero. Two of the timers, timer2 and timer3, can be set up to automatically start periodic DMA operations for DMA channels 0 and 1, respectively, without using the processor interrupt mechanism.

3.5 LEDS

The CPCI-811 has six green LEDs and one blue LED. The four green LEDs labeled, IOP, ACT, STAT0, and STAT1 are under software control. The LEDs are controlled by a write-only register which is located at address FF20 0000H. The LED Register bitmap is shown in Figure 3-1.

The remaining two green LEDs are associated with the serial ports and indicate the line interface selected, i.e. V.35 or EIA-530A. Refer to section 3.11.3 for additional information.

The blue LED is used for Hot Swap operations. Refer to section 3.13 for additional information.

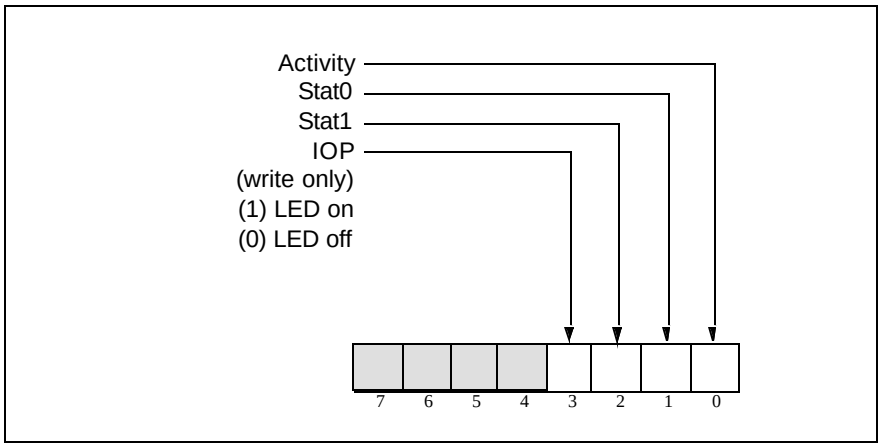

Figure 3-1. LED Register Bitmap, FF20 0000H

3.6 PCI INTERFACE

The CPCI-811 contains a primary 64-bit PCI bus and a secondary 32-bit PCI bus. Both buses are clocked at 33 MHz. The primary PCI bus interfaces the 64-bit CompactPCI bus to the 21554 PCI-to-PCI bridge. The secondary side of the 21554 interfaces a 32-bit PCI bus to the MPC8240 and the PCI9080 bridge, which interfaces the Hitachi SCAs.

3.6.1 Primary PCI Arbitration

The primary PCI bus arbitration is provided by host of the CompactPCI system.

3.6.2 Secondary PCI Arbitration

Secondary bus arbitration logic, between the MPC840 processor, the 21554 bridge and the PCI9080 bridge is contained within the MPC8240. The bus arbitration unit allows fairness as well as a priority mechanism. A two-level round-robin scheme is used, in which each device can be programmed within a pool of high- or low-priority arbitration. One member of the low-priority pool is promoted to the high-priority pool. As soon as it is granted the bus it returns to the low-priority pool.

3.7 DMA CHANNELS

The MPC8240 processor features two DMA channels. Data movement occurs on the PCI and/or memory bus. Each channel has a 64-byte queue to facilitate the gathering and sending of data. Both the local processor and PCI masters can initiate a DMA transfer. Some of the features of the MPC8240 DMA unit include: misaligned transfer capability, scatter gather DMA chaining and direct DMA modes, and interrupt on completed segment, chain, and error. Figure 3-2 provides a block diagram of the MPC8240 DMA unit.

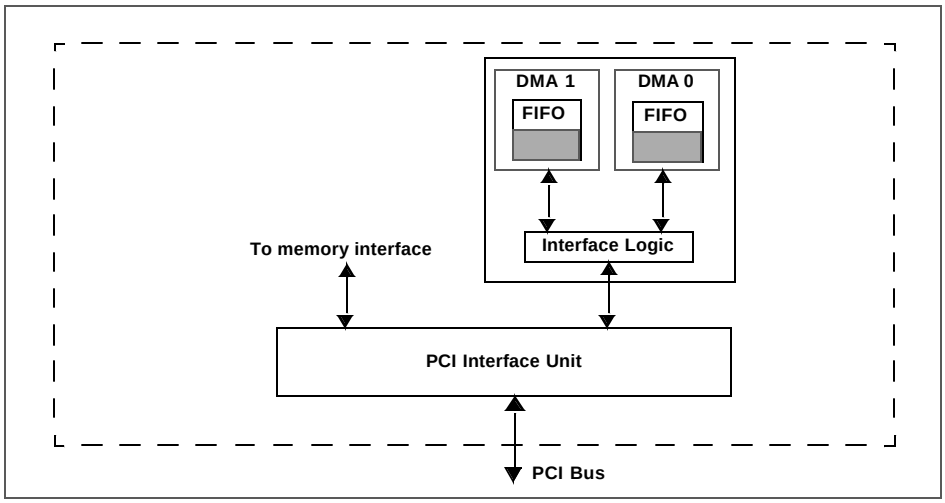

Figure 3-2. MPC8240 Processor DMA Controller

3.8 MESSAGE UNIT

The MPC8240 provides a message unit (MU) to facilitate communications between the host processor and peripheral processors. The MPC8240's MU can operate with generic messages and doorbell registers, and also implements an I_2O compliant interface.

The Intelligent Input Output (I_2O) specification allows architecture-independent I/O subsystems to communicate with an OS through an abstraction layer. The specification is centered around a message-passing scheme. An I_2O-compliant peripheral (IOP) is comprised of memory, processor, and input/output devices. The IOP dedicates a certain space in its local memory to hold inbound (from the remote processor) and outbound (to the remote processor) messages. The space is managed as memory-mapped FIFOs with pointers to this memory maintained through the MPC8240 I_2O registers. Please refer to the MPC8240 User's Manual for I_2O register descriptions, FIFO descriptions and an I_2O message queue example.

3.9 JTAG/COP SUPPORT

The MPC8240 provides a joint test action group (JTAG) interface. Additionally, the JTAG interface is used for accessing the common on-chip processor (COP) function of PowerPC processors. The COP function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor. The 16 pin COP header (sample part is Samtec # HTSW-108-07-S-S) is located at J4. The COP header adds many benefits including breakpoints, watchpoints, register and memory examination/modification and other standard debugger features. The COP header definition is shown in Table 3-3. The location of pin 1 on the header is indicated by the "cutoff" outline corner, which is shown diagonally across from the J4 designator in the silk screen, as in Figure 3-3.

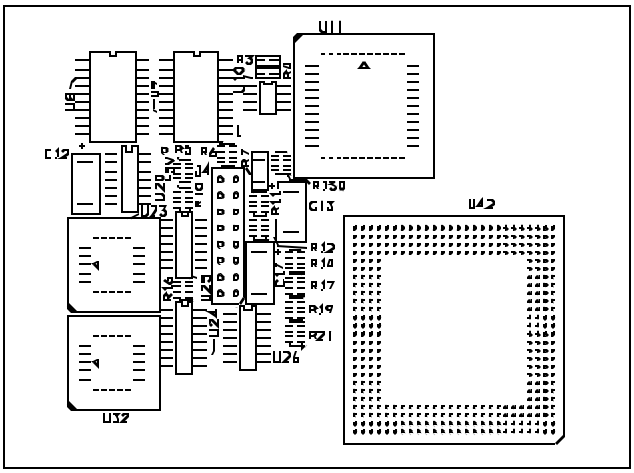

Figure 3-3. JTAG/COP Header Orientation

Table 3-3. JTAG/COP PIN ASSIGNMENT

Signal	Pin	Pin	Signal
TDO	1	2	QACK#
TDI	3	4	TRST#
Pull-up to +3V	5	6	+3V
TCK	7	8	CHKSTOPIN#
TMS	9	10	N/C
SRESET#	11	12	GND
COP_RESET#	13	14	N/C
Pull-up to +3V	15	16	GND

3.10 GEOGRAPHIC ADDRESSING

CompactPCI backplanes that support 64-bit connector pin assignments are required to provide a unique differentiation based upon which physical slot the board has been inserted. The CPCI-811 makes this definition available to the software. The definition for GA[4:0] is shown in Figure 3-4

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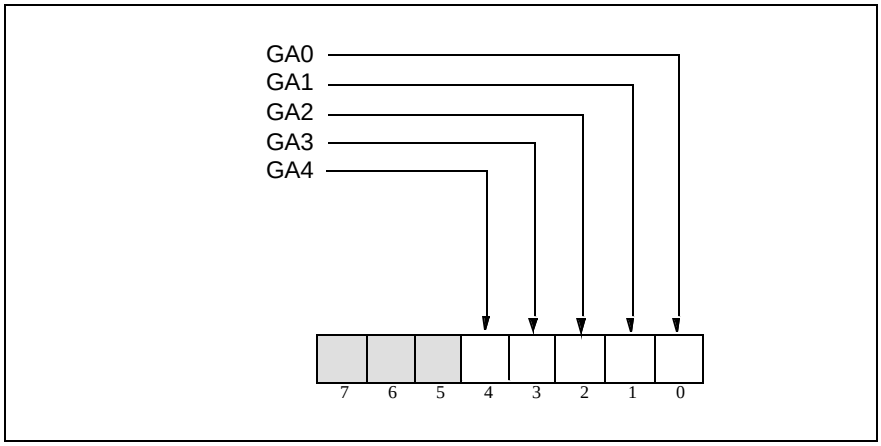

Figure 3-4. Geographic Addressing Register, FF60 0000H.

3.11 SERIAL PORTS

The four or eight high speed serial ports are based on the Hitachi HD64570 Serial Communications Adapter (SCA). Each adapter services two ports. A multiprotocol transceiver is used to switch between a V.35 line interface or an EIA-530A line interface.

3.11.1 Hitachi SCA

The HD64570 is clocked at half the host's clock rate and divides this clock internally to generate baud rates. (Normally the CompactPCI bus is clocked at 33MHz, so the SCA will be clocked at 16.5 MHz.). All ports support synchronous and asynchronous communications with many different modes and encoding/decoding, such as NRZ, NRZI, FM, SDLC/HDLC and others. Each port has 32 byte FIFOs for the transmit and receive channels.

The SCA has been configured to Big Endian byte ordering by setting the HD64570 mode pins <CPU1,CPU0> to <1,1>. The HD64570 User's manual calls this "CPU Mode 3". When reading the HD64570 User's manual, refer to tables, text, and figures for CPU Mode 3.

3.11.2 Serial Port Signaling

The line interface of the CPCI-811 serial ports is software selectable between V.35 or EIA-530A. The default (power-on reset) state is for an EIA-530A line interface. An access (Read or Write) to [PCIBAR2 + 4000H] will toggle the EIA-530A interface off and the V.35 interface on. An access to [PCIBAR2 + 5000H] will toggle the V.35 interface off and the EIA-530A interface on. A pair of green LEDs located on the front panel of the CPCI-811 provide a visual indication of the selected line interface. Note that all eight (or four) serial ports will change, one cannot set the signaling type on a port-by-port basis.

In V.35 signaling, the higher speed signals (clock and data) are transmitted differentially (balanced) while the slower control signals (such as Request to Send and Clear to Send) are transmitted single ended (unbalanced). Line termination in V.35 uses a "Y" configuration of 50 ohms from each side of a differential signal to a 125 ohm resistor to ground, at both the generator and receiver ends of the line. EIA-530A signaling uses differential (balanced) pairs for all signals. EIA-530A is terminated with 100 ohms across the differential pair at the receiver only.

3.11.3 Serial Port LEDs

A pair of green LEDs located on the CPCI-811 provide a visual indication of the selected line interface. The LED labeled "V.35" will be on when the V.35 interface has been selected and the LED labeled "530A" will be on when the EIA-530A line interface has been selected.

3.11.4 Serial Port Connector

The serial port connectors on the CPCI-811 are the Alt-A 26 position connectors found in EIA/TIA-530A. The EIA-530A standard also assigns the differential signals of EIA-422 to the connector. The CPCI-811 uses the DTE (Data Terminal Equipment) pin assignments of EIA-530A for all the signals. The single ended signals of V.35 are assigned to their respective non-inverting signal pin from EIA-530A. Table 3-4 provides a complete list of the signal assignments to the 26 position connectors, including signaling type, signal direction and corresponding ISO-2593 (V.35) connector pin assignment.

Table 3-4. Serial Port Connector Pin Assignments

Pin	CCITT Number	V.35 Pin	CPCI-811 Signal	Direction	Description
1	--	A	SHIELD	--	Chassis Ground
2	103	P	TXDA	Output	Transmit Data
3	104	R	RXDA	Input	Receive Data
4	105	**	RTSB	Output	Request to Send
5	106	**	CTSB	Input	Clear to Send
6	--	--	--	--	Not Used
7	102A	B	GND	--	Signal Common
8	109	**	DCDB	Input	Received Line Signal Detector
9	115	X	RXCB	Input	Receiver Signal Timing Element
10	109	F	DCDA	Input	Received Line Signal Detector
11	113	W	TXCB	Output	Transmit Signal Timing Element (DTE Source)
12	114	AA	TXCB	Input	Transmit Signal Timing Element (DCE Source)
13	106	D	CTSA	Input	Clear to Send
14	103	S	TXDB	Output	Transmit Data

15	114	Y	TXCA	Input	Transmit Signal Timing Element (DCE Source)
16	104	T	RXDB	Input	Receive Data
17	115	V	RXCA	Input	Receiver Signal Timing Element
18	--	--	--	--	Not Used
19	105	C	RTSA	Output	Request to Send
20	--	--	--	--	Not Used
21	--	--	--	--	Not Used
22	--	--	--	--	Not Used
23	--	--	--	--	Not Used
24	113	U	TXCA	Output	Transmit Signal Timing Element (DTE Source)
25	--	--	--	--	Not Used
26	--	--	--	--	Not Used

** These signals are not used in V.35 (DCD, CTS and RTS are single ended in V.35).

3.11.5 Serial Port Transmit Clock Direction

The direction (Input or Output) of the serial ports transmit clock is software selectable. Although the SCAs allow both their transmit and receive clocks to have an input or output direction, the CPCI-811 only allows the transmit clock to have a selectable direction, the receive clock is always an input to the serial ports. The default (power-on reset) state of the transmit clock is an output. An access (Read or Write) to [PCIBAR2 + 7000H] will change the transmit clock to an input. An access to [PCIBAR2 + 6000] will change the transmit clock back to an output. Note that all eight (or four) serial ports will change, one cannot set the transmit clock direction on a port-by-port basis.

3.12 I^2C BUS

The CPCI-811 has two temperature sensors attached to the Inter-Integrated Circuit (I^2C) bus interface of the MPC8240 processor. The I^2C addresses of the devices are shown in Table 3-5.

Table 3-5. I^2C Device Addresses

Designator	Device	Function	Address
U10	LM75	Temperature Sensor	1001000
U21	LM75	Temperature Sensor	1001001

3.12.1 Temperature Sensors

The LM75 temperature sensors have overtemperature trip points that will trigger an interrupt when crossed. The sensors have been placed on the board at U10 and U21, and share serial interrupt #5. The sensors should be placed in the interrupt mode by initialization code. The sensors can be read for a temperature reading at any time, and reading after an interrupt clears the interrupt. The sensor will not interrupt again until the temperature has dropped below the hysteresis. Consult the LM75 data sheet for more details on programming the temperature sensors.

3.13 HOT SWAP

The CPCI-811 is a PICMG 2.1 compliant Hot Swap board. The CPCI-811 is a "Full Hot Swap" board, with both Hardware and Software Connection control. The CPCI-811 can be used on all platform types; Non-Hot Swap platform for a conventional system, Hot Swap platform for a Full Hot Swap system and on High Availability platform for a High Availability system. See the Hot Swap specification for further explanation of platform, board and system types.

3.13.1 Hot Swap Extraction Process

Removal of the CPCI-811 in a Full Hot Swap or High Availability system is the same. The operator first only opens the ejector handles of the board. A switch on the CPCI-811 signals to the system that it is to be extracted. In response, the system will illuminate the blue Hot Swap LED when extraction is permitted.

3.13.2 Hot Swap Insertion Process

Insertion of the CPCI-811 is the same in any Hot Swap system. The operator merely slides the CPCI-811 into the desired slot and latches the handles.

3.14 BOARD ID REGISTER

The Board ID Register is a read-only register that can be used to differentiate between the CPCI-811 and other Cyclone Microsystems MPC8240-based CompactPCI cards. It is located at address FF70 0000h on all such cards, with each card returning a unique ID value. Figure 3-5 shows the board ID for the CPCI-811.

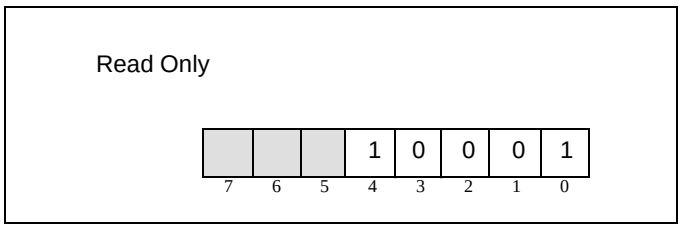

Figure 3-5. Board Identification Registers, FF70 0000h